K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

INDUSTRY INSTITUTE INTERACTION CELL

&

DEPARTMENT OF CCE & CSE (ICB)

Expert Talk on

"Disruptive technologies shaping the future"

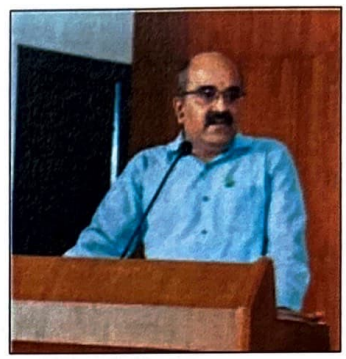
Date of Conduction: 21st December 2023

Venue: KSIT Seminar Hall, Ground Floor

Time: 10.30AM – 12.00PM

Duration: 1.30Hours

Sponsoring Bodies / Associating Organization: NA



Expert Details – with photo

Name: Shri. R. Anantharaman

Designation: Senior Advisor; Founder & CEO

Organization: Arthur D Little India & Scalepro Bengaluru

Brief Profile about the Expert:

Shri. R. Anantharaman, currently working as Senior Advisor at Arthur D Little India; and Founder & CEO - Scalepro Bengaluru. He has 32 years of remarkable leadership experience in P/L Management, Revenue enhancement, Sales & Distribution management, Marketing, Human Resource, Supply Chain, Finance, Legal, and Customer Services. In the telecom and academic industries, he has 24 years of experience, which allowed him to be at the forefront of introducing next-generation technologies since the early days of the telecom revolution in India. Additionally, he has actively participated in various process and quality improvement efforts, such as ISO certification, Six Sigma implementation, and Quality councils. Furthermore, He possess over three years of experience in academic initiatives, including entrepreneurship skilling and education for students and faculty members, livelihood development programs for women, Self Help Groups, and unemployed youths.

Description of the Event:

Disruptive technology is an innovation that significantly alters the way that consumers, industries, or businesses operate. It displaces a well-established product or technology, creating a new industry or market. One of the key features of disruptive technology is its ability to offer consumers new and notable benefits. Even a startup with limited resources can aim at technology disruption by inventing an entirely new way of getting something done. Established companies tend to focus on what they do best and pursue incremental improvements rather than revolutionary changes. They cater to their largest and most demanding customers. Some examples of disruptive technologies include Block chain Technology, Artificial Intelligence (AI), 5G Technologies, Internet of Things (IoT), Drone Technology, 3D Printing, e-commerce, GPS system and many more.

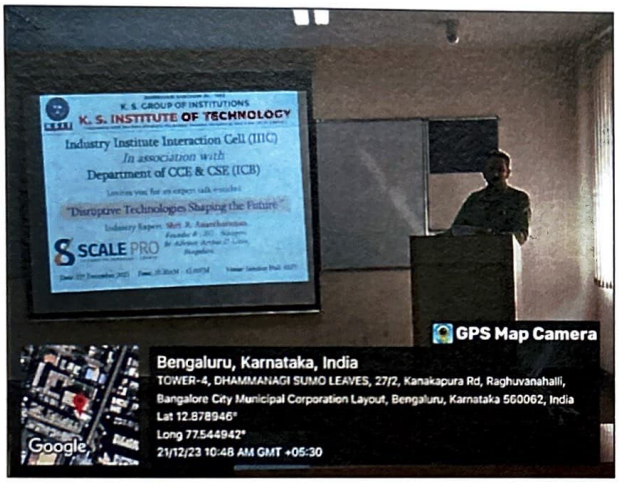
In order to understand the role and benefits of disruptive innovations in entrepreneurship journey of students, Industry Institute Interaction Cell (IIIC) in association with Department of CCE & CSE (ICB) organized an expert talk on the said title for 3rd semester students on 21st December 2023 at seminar Hall, KSIT. As per the directions of Head, Department of CCE & CSE (ICB), 3rd Semester students assembled in seminar hall at 10.25AM. The program started with welcoming the industry expert Shri. R. Anantharaman with a bouquet by Dr. Dilip Kumar K, Principal-KSIT. Mr. Rajesh G.L, Chief coordinator – IIIC outlined the meaning of disruptive technology with examples. Industry expert briefed about key features of disruptive innovation and its ability to offer consumers new and notable benefits. He also explained disruptive technologies including Block chain Technology, Artificial Intelligence (AI), 5G Technologies, Internet of Things (IoT), Drone Technology, 3D Printing, e-commerce, GPS system and many more. Further, program ended with vote of thanks by Mr. Rajesh G.L at 12.00PM.

Objectives / Key Highlights:

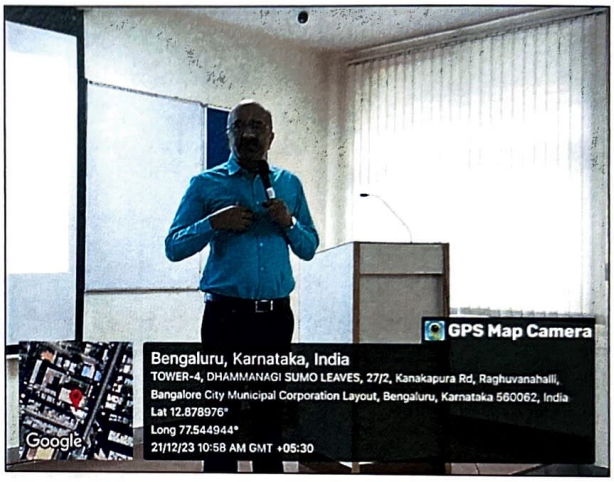
- Understand the role and benefits of disruptive innovations in young minds.
- Explore different types of disruptive technologies and its applications

Participant details - **No. of Participants: 94**
Students (internal/external): Internal (CCE – 46; CSE ICB – 48)
Faculty: Prof. Rachana, Asst. Prof. CSE (ICB) & Prof. Shashikala, CCE

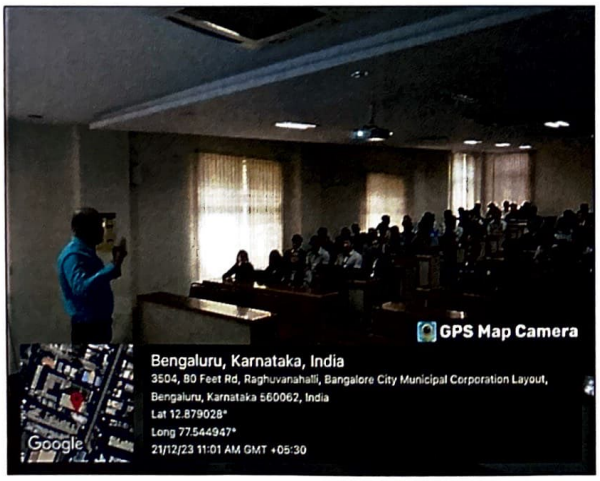
Photos (Geo Tagged):



Welcome address by Mr. Rajesh G.L



Industry expert briefing about disruptive technology



Explaining about innovation and its benefits

Students interaction with the expert

Outcomes / Benefits:

- Students understood the need of disruptive innovation for a successful entrepreneurship journey
- Explored on case studies pertaining to block chain, IoT, 5G Technology and AI.

Attachments:

1. **Communication with Resource person**
2. **Resource person Profile**
3. **Evaluation and Feedback**

CO/PO&PSO mapping - CCE

CO/PO&PSO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO 2
Expert Talk	-	-	-	-	01	-	-	-	-	-	-	-	01	-
Average	-	-	-	-	01	-	-	-	-	-	-	-	01	-

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PSO1: Ability to apply the fundamental concepts of Artificial Intelligence and Machine Learning to design and develop solutions to multidisciplinary problems of social concern.

CO/PO&PSO mapping – CSE (ICB)

CO/PO&PSO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO 2
Expert Talk	-	-	-	-	-	-	-	-	-	-	-	01	01	01
Average	-	-	-	-	-	-	-	-	-	-	-	01	01	01

PO12: Lifelong learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PSO1: Graduates will demonstrate the technical skills to address real-world challenges in IoT, cyber security, and blockchain technology while upholding ethical considerations and social responsibility.

PSO2: Graduates will engage in continuous learning, collaborate cross-functionally, and adeptly create and implement inventive solutions for societal benefit while ensuring digital security and privacy.

Mr. Rajesh G.L
Chief Coordinator - IIIC
Industry Institute Interaction Cell (IIIC)
K. S. INSTITUTE OF TECHNOLOGY
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Dr. Chanda V Reddy
Head - CCE
Head of the Department
Dept. of Computers and Communication Engg
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Dr. Ganga Holi
Head – CSE (ICB)
Head of the Department
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Cyber Security, Blockchain Tech.
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Dr. Dilip Kumar K
Principal, KSIT
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K.S.INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

DEPARTMENT OF
COMPUTER & COMMUNICATION ENGINEERING

REPORT
Technical Talk on

"ON Beyond Wires And Waves -Internet Communication & Networking Protocols Demystified "

Date of conduction: 11 January 2024

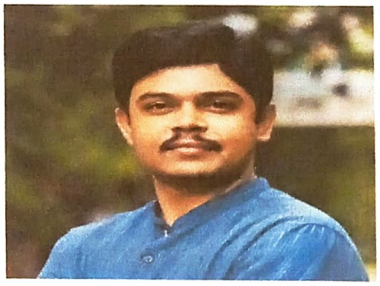
Venue: KSIT Conference hall, Ground Floor

Time: 10:30AM - 12:30 PM

Duration: 2 Hours

Sponsoring Bodies/ Associating Organization: NA

Expert details — with photo



Name: Mr.Akhil Mohan

Designation: Solution Architect

IT Organisation : Akamai Technologies

Brief Profile about the Expert:

Mr.Akhil Mohan, is a Telecommunications Engineer (2013 batch), graduated from KSIT, Bangalore. Akhil is currently working as **Solution Architect** at Akamai Technologies, a leading CDN company. He is an **AWS Certified Solutions Architect Professional**, **Google Certified Professional Cloud Architect**, and **Cisco Certified Network Associate (CCNA)**.

Being an active individual who has a craving for innovation, he has participated and won multiple national level and state level awards during his engineering days. He was awarded the first place in state level for his innovative idea on a device which can write on air. Teaching is his passion and Physics and Cloud Computing is his subject of interest. He has taught JEE-Physics for 11th and

12th standard students at Christ PU college and MCC PU college in Bangalore. He follows Indian economy, and Finance.

Description of the Event:

The internet is not really radio waves, even though it can be carried that way. If you happen to have internet through a microwave service, then that is in fact the way you receive it. The way most people get internet is though cable. Cable does have a single wire running down the middle of it that carries the radio signal than encodes the bits that comprise what we know of as the Internet. You know it comes in as a radio wave because you need a modem to see it. A modem is a radio device that modulates and demodulates the radio waves that carries the TCP IP signal that our computer interprets for us as the Internet. The fact that a lot of information can be carried on that small wire is just a fact of physics. The higher the frequency radio wave you use, the more information you can cram into it. Light waves are much higher frequency than radio waves, and once we all get fiber to our homes we will be amazed at how fast it is. Those optical fibers are hair-thin, but again, it's just a matter of wavelength that gives it that power to carry information.

A network protocol is a set of established rules that specify how to format, send and receive data so that computer network endpoints, including computers, servers, routers and virtual machines, can communicate despite differences in their underlying infrastructures, designs or standards.

Objectives / key highlights:

- Understanding about the **Wires and Waves – Internet Communication**
- Building the knowledge about **Networking Protocols Demystified**

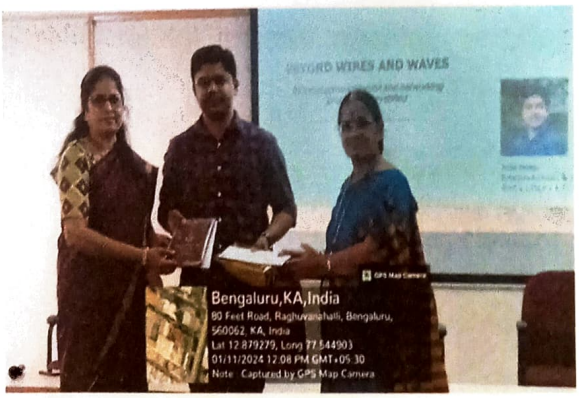
Participant details:

- No. of participants in total: 53
- Students of CCE Dept.-53
- Faculty: Prof.Nagajyothi. (CCE)
- Faculty: Prof.Shashikala.H.(CCE)

Photos:

Addressing the gathering by Principal

Talk on beyond wires and waves Internet Communication



Presenting memento to the guest

Students listening to technical talk

Outcomes/Benefits:

- Students understood about the Wires and Waves- Internet Communication.
- Students gained the knowledge on the networking protocols.

Attachments:

1. Communication with Resource person
2. Resource person Profile
3. Evaluation and Feedback

CO/PO&PSO mapping -CCE

CO/PO& PSO	PO1	P02	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Event (Technical Talk)	-	-	-	-	-	02	-	-	-	02	-	02	02	-

PSO1: To understand and apply the concepts to design and develop solutions in computer and communication Engineering.

PSO2: To use the inculcated experiential learning for research and develop inventive solutions for societal benefit while ensuring security with moral values and ethics.

T. Naga Jyothi
Event Coordinator

Dr. Chanda V. Reddy
Head - CCE

Head of the Department
Dept. of Computers and Communication Engg.
K. S. Institute of Technology
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Dr. Dilip Kumar K
Principal, KSIT

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K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

DEPARTMENT OF COMPUTER AND COMMUNICATION ENGINEERING

Report on Workshop

"VERILOG HDL"

Date of Conduction: 18th and 19th January 2024

Venue: KSIT Online lab, 4thFloor

Time:10:00AM –4:00 PM

Duration: 14 Hours.

Expert Details – with photo

Name: Padmanaban K.

Designation: Software Enabling &Optimization Engineer,

Organization: Intel Technologies India PVT. LTD.,

Place: Bangalore

Brief Profile about the Expert:

Padmanaban has been working as the Software Enabling and Optimization Engineer in the Customer Experience Group at Intel PSG for the past 3 years. He is the academic ambassador for the Intel India FPGA University Program. Padmanaban has a postgraduate degree in Applied Electronics from Anna University, Chennai, and a Bachelor in EEE from GCT, Coimbatore. He has 16+ years of experience in digital design for both FPGA and ASIC. Prior to joining Intel, he worked as a Chief Faculty in Sandeepani School of VLSI design (Training division of CoreEL Technologies, Bangalore) for 8 years and as an Assistant Professor and Project Coordinator at Ramaiah University of Applied Sciences (RUAS) Bangalore for 5 years

Sl. NO	Contents
1	Aim of the workshop
2	Abstract of the workshop
3	Introduction to basics of Digital System
4	Design in details Description Design of Describe System Hardware Description Languages Logic Simulations Things which can & can't be translated. The Role of HDL Design Methodologies &Types of HDL Verilog HDL vs. VHDL
5	Verilog HDL & its history Verilog Data Types in Details Operators, Procedural Constructs, Event-Control &Loop Statements
6	Verilog Module Description &Test Benches Verilog Modelling in Details
7	Main points to remember & some tips for Verilog HDL Coding
8	Conclusion Question &Answer (QNA)Session Practical example on computer
9	Experience from the workshop session.

Objectives / Key Highlights: To make the students

- To understand about the Verilog HDL.
- To Analyze, Synthesize, and Simulate Lab Programs.
- To execute the Lab programs using ModelSim software.

Participant details - No. of Participants: 50
Students (internal):45
Faculty: 5

1. Aim of the workshop

1). To make the students to understand about the Verilog Hardware Description Language (which is included as a part of Digital Design and Computer Organization (1BCS302) in the III semester).
2). To provide an interactive session with the industry people.
3). To create an aware of the importance of co-curricular activities in engineering domain

2. Abstract of the workshop session

Initially session dealt with the basic concepts of digital system design. Then the concepts of Verilog HDL were related with C Programming & complete details on Verilog HDL with examples were discussed.

3. Introduction to Basics of Digital System

The construction of different systems, the designs which are nothing but the specification of requirement, difference between small devices (like flip-flops) & large circuit (like microprocessors).
The hardware description languages are used to design the large & advanced circuit such as micro-controllers & microprocessors etc.The usage of the variable, constants & logics etc. in Verilog HDL are similar to C Language.

4. Design in Details

Design is the specification of requirement as discussed earlier. Design can be of different levels such as:

1. SwitchLevel
2. Register Transfer Level
3. Instruction Set Architecture Level etc.

For the design to check whether it is working or notA. Simulation& B.Synthesis isdone.

Description:

Ifthe simulation is successfullthenthe design is working & then it canbe synthesized wherethenetlistiscreated.Thisnetlistgivesoutthelistofthe components to be used.

Design of Describe System:

Thevery1st stepafterthedescriptionofsystemis howtodesignthe describe system. It includes:

- DesignSpecification
- DesignSimulation
- DesignSynthesis

Hardware Description Language:

A **hardware description language (HDL)** is a specialized computer language used to describe the structure and behavior of electronic circuits, and most commonly, digital logic circuits.
A hardware description language looks like a programming languagesuchasC; it is a textual description consisting of expressions, statements and control structures. One important difference between most programming languages and HDLs is that HDLs explicitly include the notion of time.
The functionalworkingofHDLis parallel way.

TheRoleofHDL :

Thelanguage helps to describe any digital circuit in the form of structural, behavioraland gate level and it is foundtobeanexcellentprogramming language for FPGAs and CPLDs.

Thusithasfollowingroles:

- Behavioral
- Structural
- Physical

DesignMethodologies&TypesofHDL:

Therearetwotypesofdesignmethods:

TopDown

Down Top

Thesearemainlybasedon Hierarchical Rank.

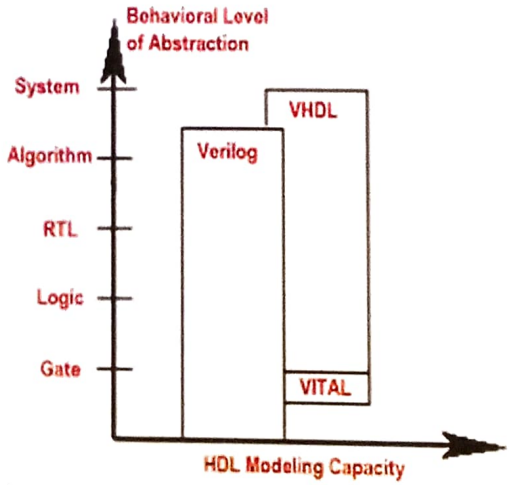
HerearemainlytwotypesofHardware Description Languageswhichare standardized by IEEE, those are as follows:

- VHDL/VHSIC HDL (Very High Speed Integrated Circuits HardwareDescriptionLanguage), is discovered by US Department of Defense
- VerilogHDL,discoveredbyOpenVerilogInternational.

VerilogHDLvs.VHDL:

WhytolearnVerilogHDLinsteadofVHDL?

- VerilogHDLgivesbetterlowendthanVHDL
- It ismoremodellinglanguage.



VHDL hasseparateinput&outputblockswhereinVerilogHDLhasbothinput & output in the same block.

5. Verilog HDL and Its History

History: Verilog HDL was invented by Phil Moor by and Prabhu Goelaround 1984. It served as a proprietary hardware modeling language owned byGateway Design Automation Inc. At that time, the language was not standardized. It modified itself inalmost allthe revisions that came out between 1984 to 1990.

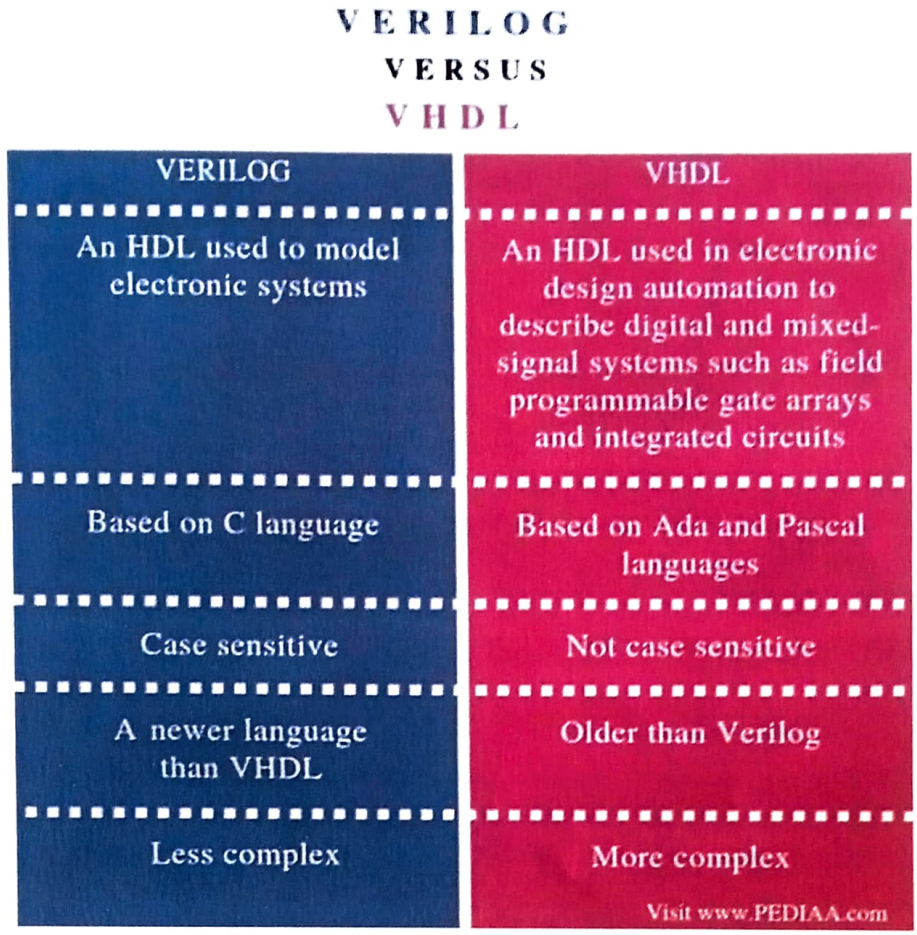


Fig:: Difference between VHDL and Verilog

6. Verilog Module

Definition: Verilog, standardized as **IEEE 1364**, is ahardware description language (HDL) used to model electronic systems.

Use: It is most commonly used in the design and verification of digital circuits at the register-transfer levelofabstraction. It is also used in the verification ofanalog circuits and mixed-signal circuits, as well as in the design of genetic circuits.

Features: Itiscasesensitive& parallel programcompilingfunction.

Verilog Data Types in Details:

Thereareprimarilytwodatatypes:

- Nets
- Registers(IntegerReal&Timer)

Nets: The internalconnections ofa block diagramexcept for input & output are called nets.Netsare represented as wires.

Registers: Thefunctionofregistersisstoringdata&showingtheresult until next input is selected,such as integers,real & timer etc.

- **Integers:**Integershavedefaultwidthof32bits.Thesearedeclaredbykeyword 'integer'.
- **Real:**Realnumber,constants&variablesare declared usingkeyword'real'.

- **Time:** Aspecialtime register data type is used in Verilog to store simulation time.
- **Arrays:**Theseareallowedforreg,integer&time,notallowedforreal variables.
- **Strings:**Canbestored inreg.Eachcharacterinstringrequires8bitsof storage.

Operators,ProceduralConstructs&LoopStatements:

Operators: Theoperatorsaresameas'C'Programmingoperatorsasshown in figure Below

1	() [] -> . ::	Grouping, scope, array/member access
2	! ~ - + * & sizeof *type cast* ++x --x	(most) unary operations, sizeof and type casts
3	* / %	Multiplication, division, modulo
4	+ -	Addition and subtraction
5	<< >>	Bitwise shift left and right
6	< <= > >=	Comparisons: less-than, ...
7	== !=	Comparisons: equal and not equal
8	&	Bitwise AND
9	^	Bitwise exclusive OR
10	|	Bitwise inclusive (normal) OR
11	&&	Logical AND
12	||	Logical OR
13	?:	Conditional expression (ternary operator)
14	= += -= *= /= %= &= |= ^= <<= >>=	Assignment operators
15	,	Comma operator

- **ProceduralConstructs:**
  - InitialStatement(Evaluateonlyonce)
  - Always Statement (Evaluate inaloopmanner)
- **LoopStatement:**
  - Repeat
  - While
  - For

Description & Test Benches:

A module represents a design unit that implements specific behavioural characteristics and will get converted into a digital circuit during synthesis.
Any combination of inputs can be given to the module, and it will provide a corresponding output.It allows the same ***module*** to be reused to form more significant modules that implement more complex hardware.

Hardware Schematic

Instead of building up smaller blocks to form bigger design blocks. the reverse process can also be done.

Consider the breakdown of a simple GPU engine into smaller components such that each can be represented as a module that implements a specific feature.

```
module <name> ([port_list]);
        // Contents of the module
endmodule
      // A module can have an empty portlist
module name;
     // Contents of the module
endmodule
```

ii.TestBenches: Implementsinglemodelformanyinput withoutwritingmanually.

Verilog Modelling in Details:

Thereare mainlythreetypesofmodellinginVerilogHDLasfollows:

- Gaatelevelmodelling(LogicGates)
- DataFlowmodelling(AssignBooleanexpressions)
- Behavioralmodelling(Result)

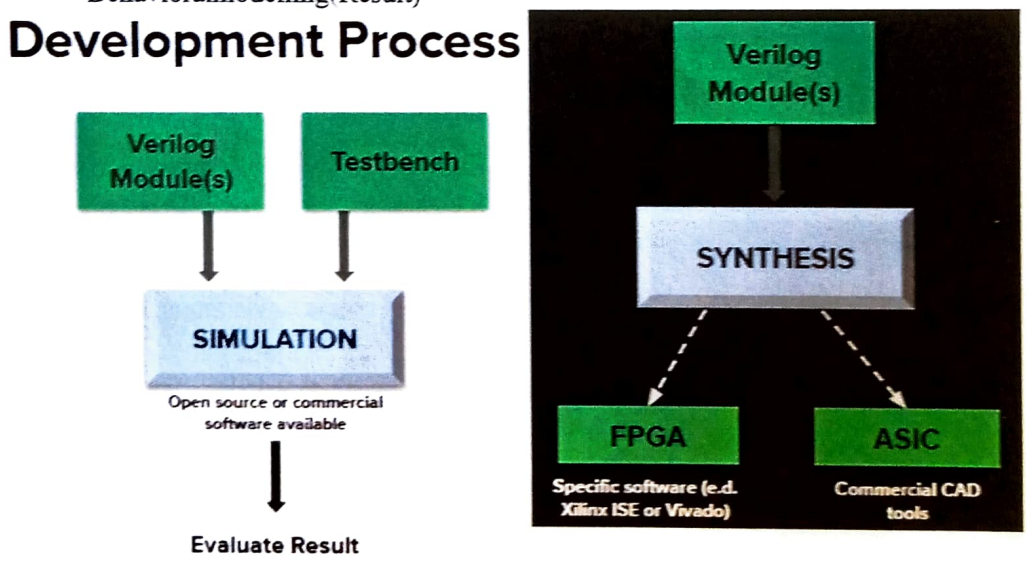


Fig: Development and Synthesis Process

7. Main points to remember & some tips for Verilog HDL Coding

Mainpointstoremember:

Verilogisconcurrent.

Thinkwhilewritingtheprogram-planforrequirement.

Blocking&UnblockingCode.

Tips:Don'ts	Does
Don'tWrite'C'code Thinkhardware,notalgorithm Verilog is inherently parallel, Compilersdon'tmapalgorithmtocircuit.	Dodescribehardwarecircuits Firstdrawadataflowdiagram Then start coding

8. Conclusion:

The sessionwas concluded withsome questions and answers & practicalcoding example in computer. I asked different questions toPadmanaban K. sir about Verilog coding's and sir cleared all the doubt with satisfactory answers.

Question & Answer (QNA)Session:

i). Whatisdone forreducingverylargecircuittransistor?

Answer: The channel length is reduced.

ii). Question:Isthe'Always'statementhassameworkedasanyotherloop?

Answer: Yes,itissimilar to 'for','while'& 'do while'loop.But themain thing to be keep in mind is conditions.

iii).Question:WhichstyleofVerilogcodingisbeingusedthemost?

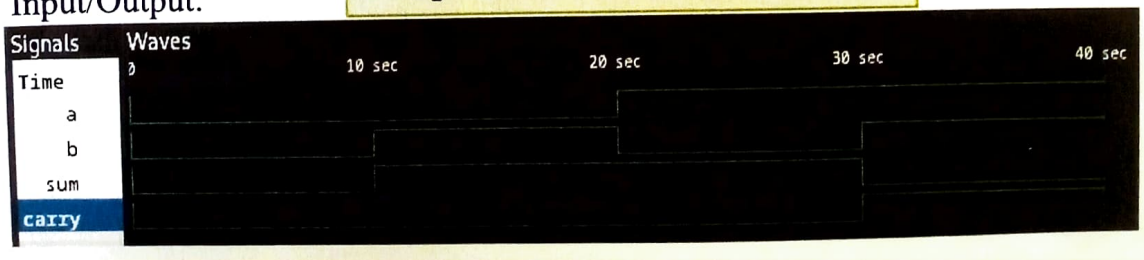
Answer: There is nothing a particular style like structural,dataflow or behavioralstyle is used,foranyspecificationthe mixedofanyofthesethreeare used.

Practical example on computer:

Ahalfadder modulecodingwas showninthreedifferentcodingstyles practically and its output.The codesare as follows:

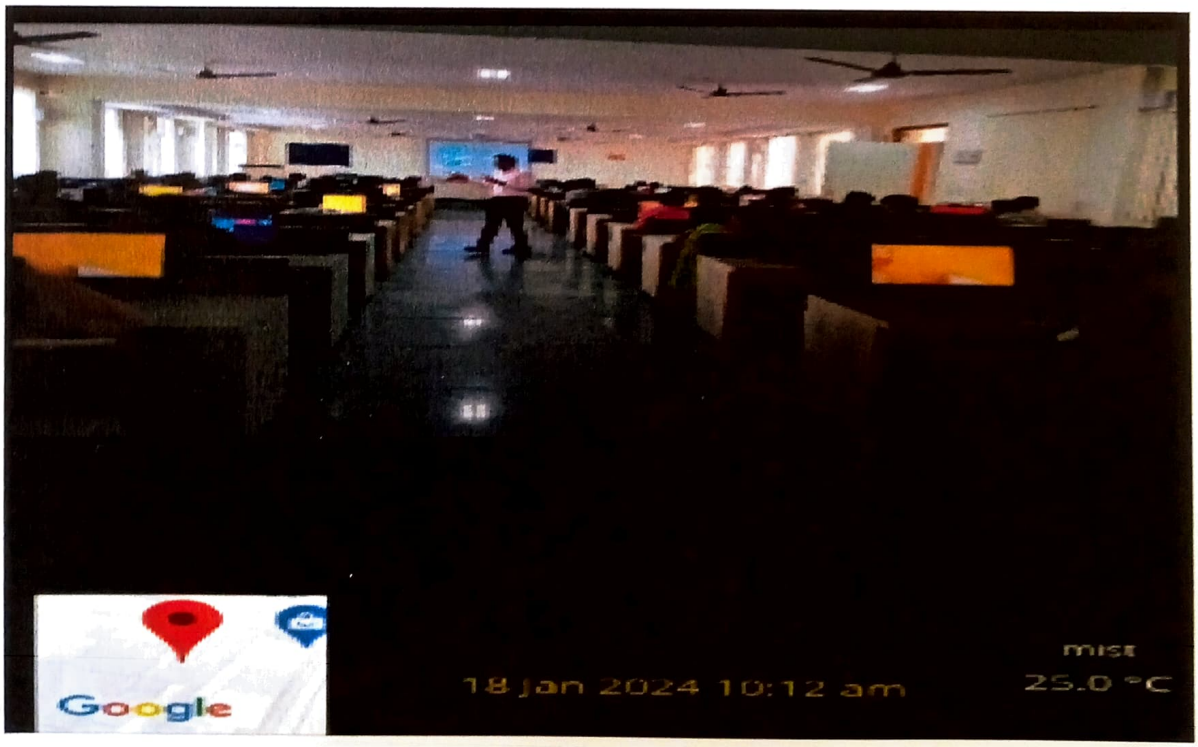
```
moudleHalf_adder(a,b,sum,carry)

//DataFlowStyle
input a,b;
outputsum, carry;

assign sum =a^b;
assigncarry =a&b;

//StructuralStyle
xor(sum,a,b);
and(carry,a,b);

//Behavioral Style
if a='0';
b='0';
then sum=0;
carry=0;
else
sum=1;
carry=0;
```

Input/Output:

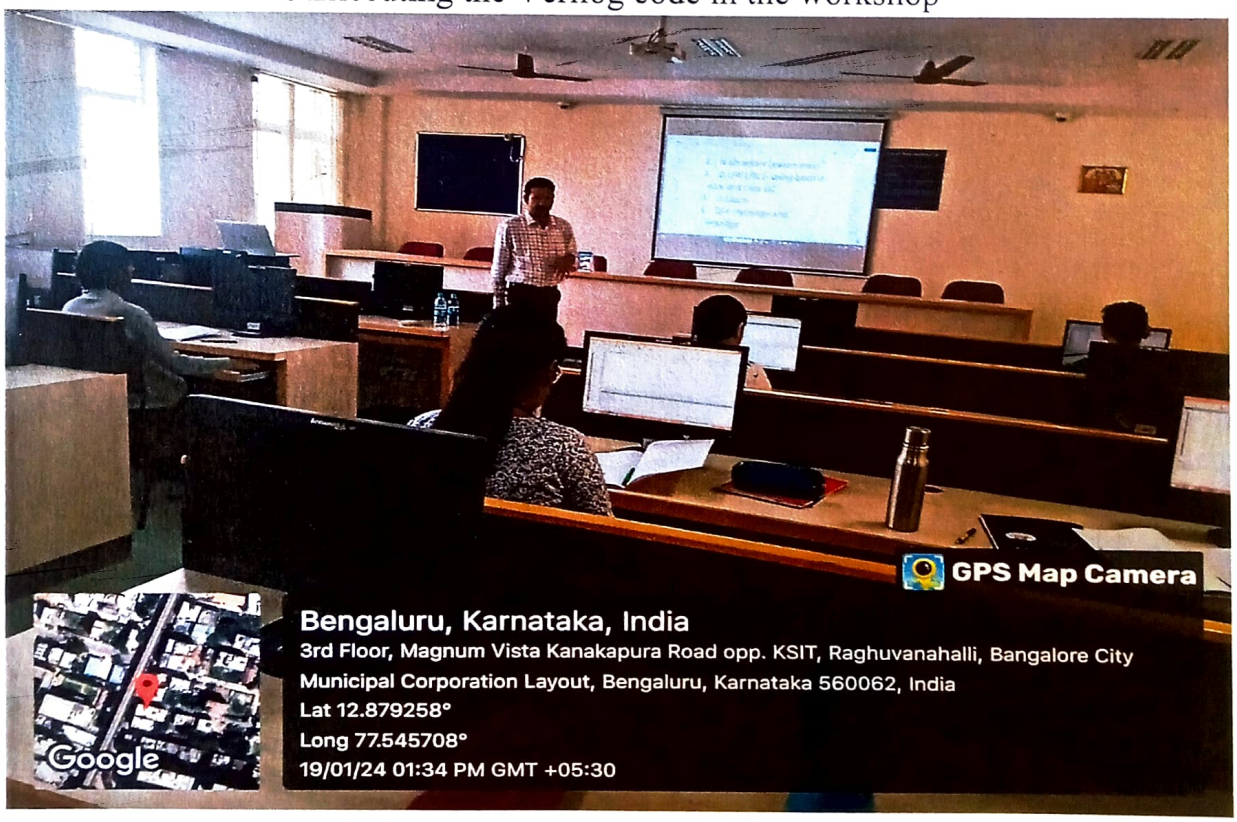


Photos:

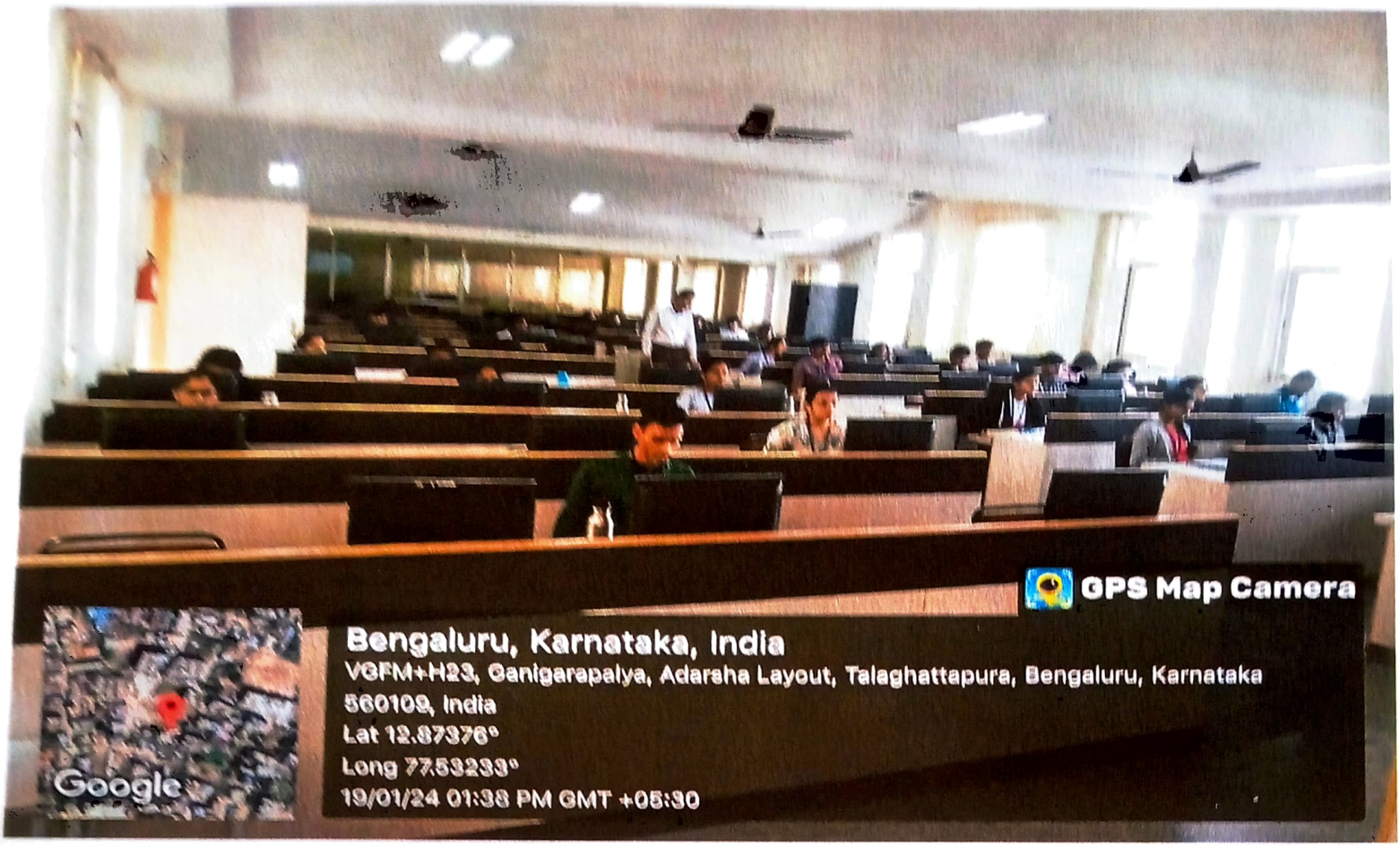
Final day photo with Principal, Padmanabhan K,HOD and students



Students Executing the Verilog code in the workshop



Students listening in the workshop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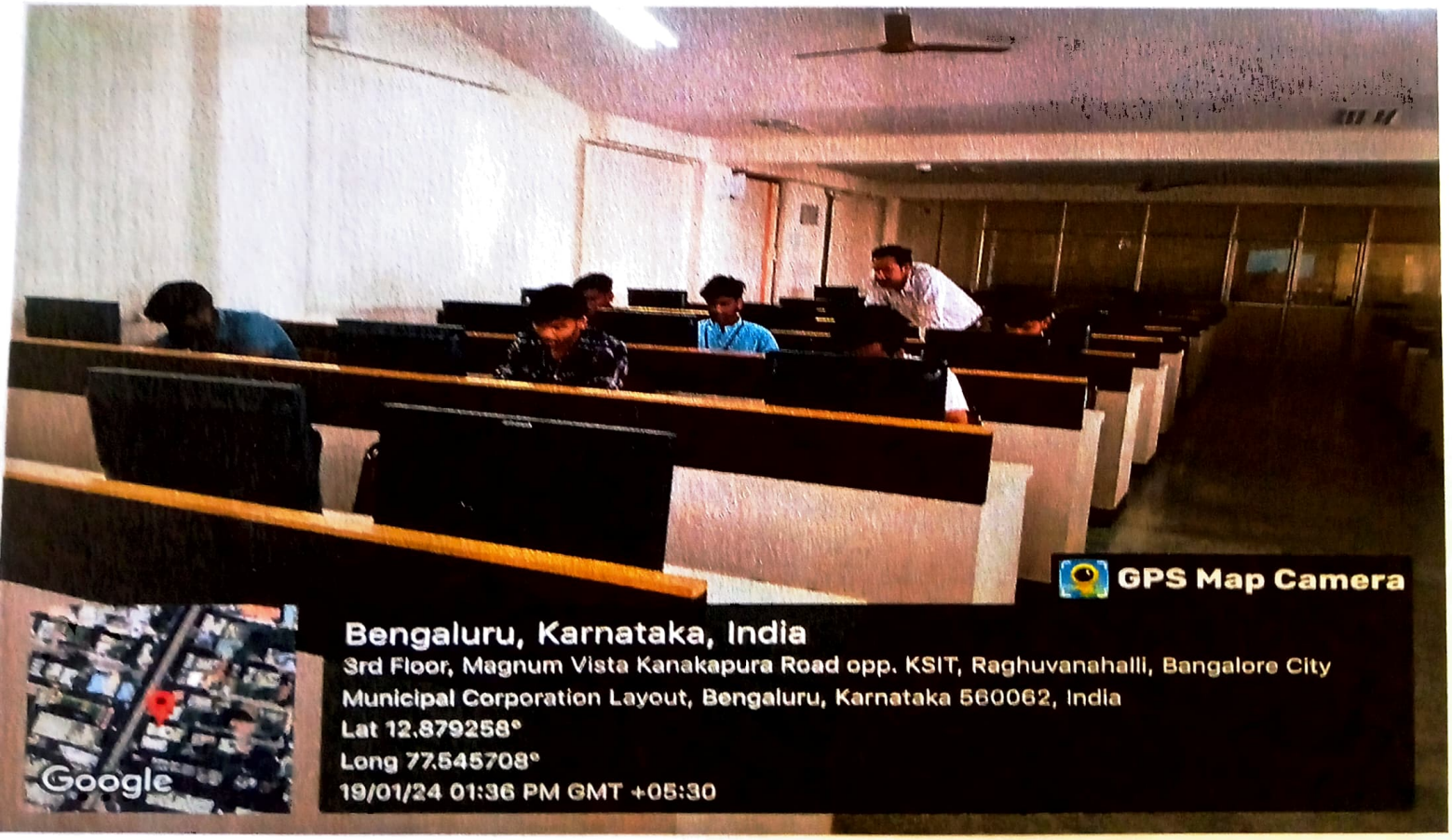
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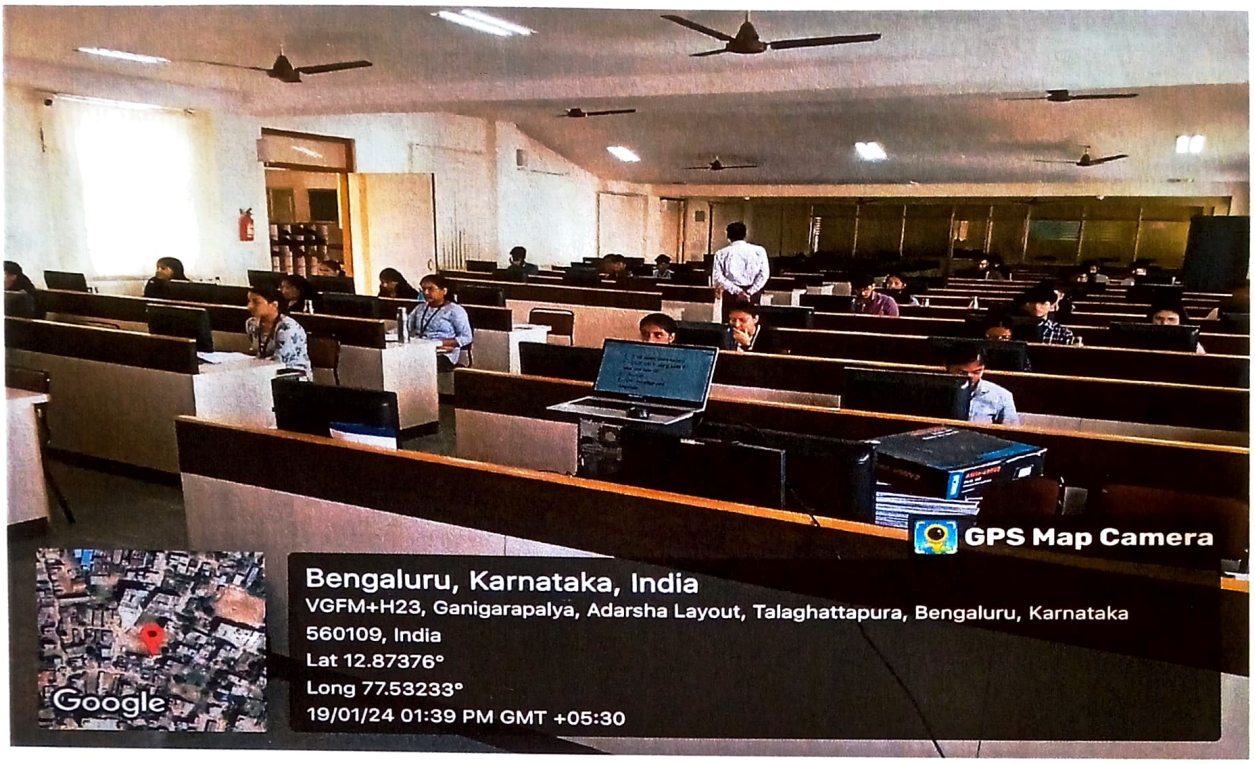
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9. Experience from the Work shop.

It was an informative, interesting and a successful workshop session. As a student of Computer& Communication Engineering, we understood the importance of Verilog HDL within Two days. I Express my thanks to Mr.Padmanaban K.who spent his valuable time for us. We also thank you to our respected Principal sir,HOD madam and our Managementfor arranging such an informative program. Finally, I would like to thank full to my colleagues and our students to make this work shop very successful.

Outcomes / Benefits:

- Studentsunderstoodaboutthe Verilog-HDL.
- Studentsgainedtheknowledgeonthe Verilog-HDL coding and Simulation.

Attachments:

1. CommunicationwithResourceperson
2. ResourcepersonProfile
3. EvaluationandFeedback

CO/PO&PSOmapping-CCE

CO/PO &PSO	PO1	P02	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Event (Workshop)	-	-	3	-	3	2	-	-	2	3	-	3	2	2

PSO1: To understand and apply the concepts to design and develop solutions in computer and communication Engineering.

PSO2: To use the inculcated experiential learning for research and develop inventivesolutions for societal benefit while ensuring security with moral values and ethics.

Shashikala H.C 30/1/24

Shashikala H.C.
Event Coordinator

30/1/24

Dr.ChandaV. Reddy
Head-CCE

Dr.DilipKumarK.
Principal, KSIT

K.S.INSTITUTE OF TECHNOLOGY, BANGALORE – 560109
DEPARTMENT OF
COMPUTER&COMMUNICATION ENGINEERING

REPORT on
INDUSTRIAL VISIT

"IOT TECH EXPO"

Date of Visit: 2/02/2024

Venue: KTPO Convention Centre
White field, Bengaluru, India
Duration: 10:00 AM- 6:00 PM

Description of the Event:

IoTshow is the premier event in india focused on the Internet of Things industry.This expo cum conference brings together industry leaders,innovators,and experts to showcase the latest technologies,products, and solutions in the IoT space.**IoTshow** is the place to be stay ahead of the curve in the rapidy evolving world of IoT.It is one of the "**India's Largest Expo Cum Conference Dedicated to IoT".**

IoT India expo showcases organizations leading the way in IoT adoption, enabling them to propel into a new world of business quicker, with more accurate data, ensuring their business can thrive through new technology adoptions. As the leading enterprise event across IoT, Blockchain, AI, Big Data, Cyber Security and Cloud, this event is a great platform for IT Professionals to meet and discuss the future of technology. From enterprise to government, SMBs to technology and service providers, it is suitable for those who are making investment and strategy decisions, or building and executing projects within their organisation.

Exhibitors for the event:

1. 99 WORLD BATER
2. AAD SOLUTECH PRIVATE LIMITED
3. AAVIZA ELECTRONICS PRIVATE LIMITED

4. ABHAS IO DEMO BOOTH
5. ADVANTECH INDUSTRIAL COMPUTING INDIA PRIVATE LIMITED
6. ALTAIR ENGINEERING INDIA PVT LTD
7. AMBIQ
8. ANRITSU INDIA PVT LTD
9. AXIS BANK
10. BEVYWISE NETWORKS LLP
11. BLUE DOT VENTURES
12. BRAIN CHILD TECHNOLOGIES
13. CHIPEDGE TECHNOLOGIES PRIVATE LIMITED
14. CHIPMAX DESIGNS PVT LTD
15. CIRCUIT ELECTRONICS
16. CIRCUIT SYSTEMS LTD
17. CONINS PUNE
18. FIDEL SOFTTECH LTD

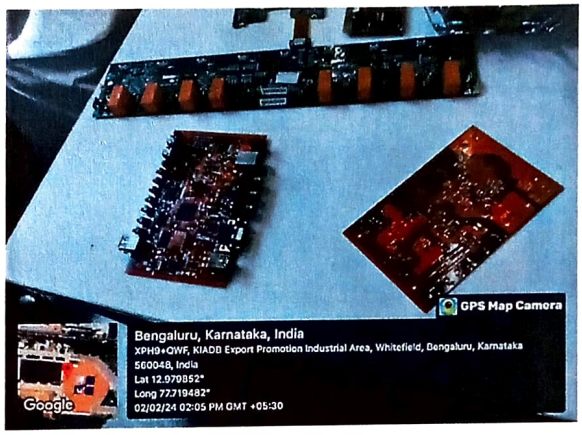
And Many More companies exhibited their products.

Objectives/Highlights :

- IoT show displays about latest technologies and products related to IoT Sensors , Automation , AI&ML.
- Displays how manufacturing units such as machines are used to insert many chips on PCB's
- Displays how IoT apps are used in healthcare domain.

No. of students attended for the event: 38 members
Faculty: T. Naga Jyothi

Photos:



CO/PO&PSO mapping -CCE

CO/PO& PSO	PO1	P02	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Event (Industrial visit)	-	-	-	02	02	02	-	-	02	02	-	02	-	02-

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T. Naga Jyothi
Event Coordinator

Dr. Chanda V. Reddy
Head - CCE

Dr. Dilip Kumar K
Principal, KSIT

Head of the Department
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Bengaluru - 560 109.