KSIT BANGLORE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE FILE

NAME OF THE STAFF	:BHARGAVI ANANTH
SUBJECT CODE/NAME	:BEC302/DIGITAL SYSTEM DESIGN USING VERILOG
SEMESTER/YEAR	: III/II
ACADEMIC YEAR	: 2023-24
BRANCH	: ECE

COURSE IN-CHARGE

HOD

K. S. INSTITUTE OF TECHNOLOGY

VISION

"To impart quality technical education with ethical values, employable skills and research to achieve excellence".

MISSION

- To attract and retain highly qualified, experienced & committed faculty.
- To create relevant infrastructure.
- Network with industry & premier institutions to encourage emergence of new ideas by providing research & development facilities to strive for academic excellence.
- To inculcate the professional & ethical values among young students with employable skills & knowledge acquired to transform the society.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VISION

"To achieve excellence in academics and research in Electronics & Communication Engineering to meet societal need".

MISSION

- To impart quality technical education with the relevant technologies to produce industry ready engineers with ethical values.
- To enrich experiential learning through active involvement in professional clubs & societies.
- To promote industry-institute collaborations for research & development.

K.S. INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES (PEO'S)

PEO1: To Excel in professional career by acquiring domain knowledge.

PEO2: To pursue higher Education & research by adopting technological innovations by continuous learning through professional bodies and clubs.

PE03: To inculcate effective communication, team work, ethics, entrepreneurship skills and leadership qualities.

PROGRAM SPECIFIC OUTCOMES (PSO'S)

PSO1: Graduate should be able to understand the fundamentals in the field of Electronics & Communication and apply the same to various areas like Signal processing, embedded systems, Communication & Semiconductor technology.

PSO2: Graduate will demonstrate the ability to design, develop solutions for Problems in Electronics & Communication Engineering using hardware and software tools with social concerns.

K S INSTITUTE OF TECHNOLOGY

PROGRAM OUTCOMES (PO'S)

Engineering Graduates will be able to:

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11; Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

K.S.INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.
LIST OF STUDENTS STUDYING IN III SEMESTER (A& B SECTIONS)
FOR THE ACADEMIC YEAR 2023 (ODD SEMESTER)

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113	1KS22EC113	VARSHINI S	F		varshinis860@gmail.com	9108378191	Shivalingegowda S L	9902872595	Savitha G D	9980691231		B
114	1KS22EC114	VARUN	M		vkul412@gmail.com	7795747512	Manohar Rao Kulkarni	9731492002	Kavita Kulkarni	9380942421		B
115	1KS22EC115	VARUN RAYAPATI R	M		varunrayapati2004@gmail.com	9972528440	Raghvendra R K	9845779800	Sindhu M L	9972528440		B
116	1KS22EC116	VEDASHREE M	F		vedashree.mmnaidu@gmail.com	9740647879	M.Munirajulu naidu	9741581738	M.Sujatha	9480064501		B
117	1KS22EC117	VIDYASHREE H	F		Vidya.jk2003@gmail.com	97427 22262	Harish.K.S	9740354909	Jyothi k s	8073924239		B
118	1KS22EC118	VIJAYKUMAR SHANMUKHAYYA NAVALAGIMATH	M		victoryprince007@gmail.com	8147258079	Shanmukhayya Navalagimath	9591418077	Rachavva Navalagimath	9591418077		B
119	1KS22EC119	VIKAS K S	M		viki39884@gmail.com	7204372952	Shivalinge gowda	7204372952	Jyothi	7204372952		B
120	1KS22EC120	VISHWANATH B S	M		vishuvishwanath2734@gmail.com	6363437082	SATHYA	7406866626	VANAJA	7899930951		B
121	1KS22EC121	VISHWANATH VEERAPUR	M		vishwanathveerapur34@gmail.com	8050229357	Mallikarjun	9686609996	Kalavati	9606128234		B
122	1KS22EC122	VISHWAS M K	M		vishwasvishwa227@gmail.com	8431712121	Kumar	9844205672	Geetha	8431712121		B
123	1KS22EC123	VIVEK M S	M		vivekishu72@gmail.com	8073973038	Murthy Mahadeva Naik .G	9482522918	S Shaila Bai	9743646525		B

124	1KS22EC124	VIVEK RAJ B	M		Vivekrajb1211@gmail.com	9902991211	Bharani kumar raju	9986250486	Sirisha b	7892195342		B
125	1KS22EC125	YASHAVANTHA S	F		yashwanthsy80@gmail.com	9019832257	Shankar.B	9019832257	Dakshayini	9019832257		B
126	1KS22EC126	YASHWANTH P V	M		yashwanthpv7022@gmail.com	7022297805	Venkatesh PV	9448054008	Subhashini	9448054008		B

III SEMESTER TIME TABLE FOR THE YEAR 2023 (ODD SEMESTER)

W.E.F. : 15/11/2023 — CLASS TEACHER : Mrs. Bhargavi Ananth

SEC : 'B' — CLASS ROOM : OB LH 203

PERIOD	1	2	10.20 AM 10.35 AM	3	4	12.25 PM 1.15 PM	5	6	7
TIME DAY	8.30 AM 9.25 AM	9.25 AM 10.20 AM		10.35 AM 11.30 AM	11.30 AM 12.25 PM		1.15 PM 2.10 PM	2.10 PM 3.05 PM	3.05 PM 4.00 PM
MON	EP&C (BEC303)	DSDV (BEC302)	TEA BREAK	NA (BEC304)	Maths (BMATEC301)	LUNCH BREAK	DSDV LAB (BEC302) - B1 / A&DSD LAB (BECL305) -B3 / EP&C LAB (BEC303) - B2		
TUE	CO&A (BEC306C)	DSDV (BEC302)		Maths (BMATEC301)	EP&C (BEC303)		LABVIEW LAB (BEC358A)		
WED	CO&A (BEC306C)	Maths (BMATEC301)		DSDV (BEC302)	NA (BEC304)		DSDV LAB (BEC302) - B2 / A&DSD LAB (BECL305) -B1 / EP&C LAB (BEC303) - B3		
THU	Maths (BMATEC301)	EP&C (BEC303)		NA (BEC304)	CO&A (BEC306C)		DSDV (BEC302)	SC&R (BSCK307)	NSS (BNSK359) /SPORTS BPEK359)/ Yoga (BYOK359)
FRI	DSDV LAB (BEC302) - B3 / A&DSD LAB (BECL305) -B2 / EP&C LAB (BEC303) - B1				CO&A (BEC306C)		EP&C (BEC303)	NA (BEC304)	NSS (BNSK359) /SPORTS BPEK359)/ Yoga (BYOK359)

Sub-Code	Subject Name	Faculty Name
BMATEC301	AV Mathematics-III for EC Engineeri	Mr. Naveen
BEC302	Digital System Design using Verilog	Mrs . Bhargavi Ananth
BEC303	Electronic Principles and Circuits	Dr. Devika B
BEC304	Network Analysis	Mr. Christo Jain
BECL305	Analog and Digital Systems Design Lab	Mr. Satish Kumar B, Mrs. Suma Santhosh
BEC306C	Computer Organization and Architecture[**Engineering Science Course Elective**]	Mrs. Priyadharshini V
BSCK307	Social Connect and Responsibility	Dr. Sangappa S B
BEC358A	LABVIEW Programming (**Ability Enhancement Course/Skill Enhancement Course– III**)	Mrs. Bhargavi Ananth , Mr. Naveen Kumar S, Dr. Electa Alice Jayarani A , Mrs. Radhika T S
BEC302	Digital System Design using Verilog **[Theory Lab]**	Mrs. Bhargavi Ananth , Mrs. Anita P , Mr. Naveen Kumar S,
BEC303	Electronic Principles and Circuits **[Theory Lab]**	Mrs. Ramya K R, Mrs. Vishalini Divakar
BNSK359	National Service Scheme (NSS)	Mr. Naveen
BPEK359	Physical Education (PE) (Sports and Athletics)	Mr. Shiva Prakash
BYOK359	Yoga	

Time Table Co-ordinator

HOD

HEAD OF THE DEPARTMENT
Dept. of Electronics & Communication Engg
K.S. Institute of Technology
Bengaluru - 560 109

Principal

PRINCIPAL
K.S. INSTITUTE OF TECHNOLOGY
BENGALURU - 560 109.

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE -109

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INDIVIDUAL TIME TABLE FOR THE YEAR - 2023 (ODD SEMESTER)

W.E.F. : 25/10/2023

NAME OF THE FACULTY : Mrs. BHARGAVI ANANTH DESIGNATION: ASSISTANT PROFESSOR

PERIOD	1	2	10.20 AM 10.35 AM	3	4	12.25 PM 1.15 PM	5	6	7
TIME / DAY	8.30 AM 9.25 AM	9.25 AM 10.20 AM		10.35 AM 11.30 AM	11.30 AM 12.25 PM		1.15 PM 2.10 PM	2.10 PM 3.05 PM	3.05 PM 4.00 PM
MON		DSDV (BEC302)-B	TEA BR			LUNCH BREAK	← DSDV LAB (BEC302) - B1 →		
TUE		DSDV (BEC302)-B					← LABVIEW LAB (BEC358A) →		
WED	← DSDV(BEC302)-B DSDV LAB (BEC302) - A2 →						← DSDV LAB (BEC302) - B2 →		
THU			EAK				DSDV (BEC302)-B		
FRI	← DSDV LAB (BEC302) - B3 →						← LABVIEW LAB (BEC358A) →		

	Subject Code	Subject Name	Sem	Section	Work Load
Subject 1	BEC302	Digital System Design using Verilog	III	B	4
Lab -1	BEC302	Digital System Design using Verilog (Theory Lab)	III	A&B	12
Lab-2	BEC358A	LABVIEW Programming (Ability Enhancement Course/Skill Enhancement Course– III)	III	A&B	6
Project	18ECP78	Project Work Phase - 1			2 +2 (Time table)
ADDITIONAL WORK: MENTORING AND OTHERS					
TOTAL LOAD= 26 Hrs/Week					

Time Table Co-ordinator

HOD

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K.S. Institute of Technology
Bengaluru - 560 109

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BENGALURU - 560 109.

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-5600109

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CO-PO MAPPING: DIGITAL SYSTEM DESIGN USING VERILOG

Course: _ Digital System Design using Verilog	**Course Code:BEC302**	**Type: IPCC**
Course In charge : Bhargavi Ananth/Naveen Kumar S	**Academic year: 2023-24**	

No of Hours per week

Theory (Lecture Class)	Practical/Field Work/Allied Activities	Total/Week	Total teaching hours
4	0	4	50

Marks

Internal Assessment	Examination	Total	Credits
50	50	100	4

Aim/Objective of the Course:

This Course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and QuineMcCluskey minimization techniques
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits..
4. To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

Course Learning Outcomes:

After completing the course, the students will be able to, Bloom's Level

BEC302.1	**Make use of** K-Maps and Quine- Macluskey Techniques to simplify the Boolean functions.	**K3[Applying]**
BEC302.2	**Make use of** Verilog operators and data types to develop the Verilog programs using data flow description style.	**K3[Applying]**
BEC302.3	**Apply** the concepts of combinational logic to build digital circuits using MSI Components and PLD'S.	**K3[Applying]**
BEC302.4	**Make use of** the concepts of flip flops to build the sequential circuits.	**K3[Applying]**
BEC302.5	**Apply** the concepts of behavioral and structural descriptions to develop Verilog programs for digital circuits.	**K3[Applying]**

Syllabus Content:

Module 1: Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. LO: At the end of this session the student will be able to,	**CO1** **8 hrs** PO1-3 PO2-3 PO3-3 PO4-2 PO5-3

1. Understand the meaning of combinational circuits 2. Generate the switching equations for the given requirement 3. Simplify the switching expression obtained so that logic circuit can be obtained with minimum number of gates	PO9 -2 PO10-2 PO12-2 PSO1-3 PSO2-2
Module2 Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) LO: At the end of this session the student will be able to, 1. Understand the designing of combinational logic circuits 2. Need of programmable logic devices for building logic circuits Building of logic circuits using PLD's.	**CO20** **8 hrs** PO1-3 PO2-3 PO3-3 PO4-2 PO5-3 PO9 -2 PO10-2 PO12-2 PSO1-3 PSO2-2
Module 3 Flip-Flops and its Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. LO: At the end of this session the student will be able to, **1.** Understand the working of different types of flip flops. **2.** Identify the characteristic equation for the flip flops **3.** Designing of sequential circuits using flip flops	**CO3** **8 hrs** PO1-3 PO2-3 PO3-3 PO4-2 PO5-3 PO9 -2 PO10-2 PO12-2 PSO1-3 PSO2-2
Module 4 Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description.) Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description LO: At the end of this session the student will be able to, 1. Understand the basics of Verilog 2. Different types of descriptions in verilog 3. Understand the structure of different types of data flow description	**CO4** **8 hrs** PO1-3 PO2-3 PO3-3 PO4-2 PO5-3 PO9 -2 PO10-2 PO12-2 PSO1-3 PSO2-2
Module 5: Verilog Behavioural description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioural Description of Multiplexers (2:1, 4:1, 8:1). (Verilog Structural description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder LO: At the end of this session the student will be able to, 1. Understand the use of sequential statements and loop statements 2. Make use of Behavioural description for designing multiplexers 3. Make use of Structural description for designing ripple carry adder	**CO5** **8 hrs** PO1-3 PO2-3 PO3-3 PO4-2 PO5-3 PO9 -2 PO10-2 PO12-2 PSO1-3 PSO2-2
Text Books: • Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001 • Digital Principles and Design by Donald D Givone, McGraw Hill, Publications • HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press	

Reference Books:

- Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
- Logic Design, by Sudhakar Samuel, Pearson/ Sanguine,
- Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

Useful websites:

- https://www.digitalelectronicsdeeds.com
- https://www.digitalsystemdesign.in
- https://www.allaboutcircuits.com

Useful Journals

- International Journal of Digital Electronics
- International Journal of Microelectronics and Digital integrated circuits
- Journal of Digital Integrated Circuits in Electrical Engineering

Teaching and Learning Methods:

1. Lecture class: 40 hrs.
2. Self-study: 4hrs.
3. Lab Sessions: 13 Lab Slots

Type of test/examination: Written examination:
Continuous Internal Evaluation(CIE) : 50 Marks

(a)Theory Component

20 marks (Average of best two tests will be considered out of three tests)
10 marks (Average of two assignment marks)

(b) Practical Component

15 marks (Average of write up and conduction of 12 lab experiments)
05 marks (Test will be conducted for 50 marks and scaled down to 05 marks)
Test Duration: 180 minutes

Semester End Exam(SEE) :50 marks (students have to answer all main questions for 100 marks and scaled down to 50)
Examination duration: 3 hrs

CO - PO MAPPING

PO1: Science and engineering Knowledge **PO2:** Problem Analysis **PO3:** Design & Development **PO4:** Investigations of Complex Problems **PO5:** Modern Tool Usage	**PO6:** Engineer & Society **PO7:** Environment and Sustainability **PO8:** Ethics **PO9:** Individual & Team Work **PO10:** Communication **PO11:** Project Management & Finance **PO12:** Life long Learning

PSO1: Graduate should be able to understand the fundamentals in the field of Electronics & Communication and apply the same to various areas like Signal Processing embedded systems, Communication & Semiconductor technology.

PSO2: Graduate will demonstrate the ability to design, develop solutions for Problems in Electronics Communication Engineering using hardware and software tools with social concerns.

CO PO Mapping details for Academic Syllabus

CO BEC302	Bloom's Level	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2
BEC302.1	K3	3	3	3	_	3	_	_	2	2	2	_	2	3	2
BEC302.2	K3	3	3	3	_	3	_	_	2	2	2	_	2	3	2
BEC302.3	K3	3	3	3	_	3	_	_	2	2	2	_	2	3	2
BEC302.4	K3	3	3	3	_	3	_	_	2	2	2	_	2	3	2
BEC302.5	K3	3	3	3	_	3	_	_	2	2	2	_	2	3	2
BEC302 (Before CBS)		**3**	**3**	**3**	_	**3**	_	_	**2**	**2**	**2**	_	**2**	**3**	**2**

CO PO Mapping details with Content Beyond Syllabus

CO BEC302	Bloom's Level	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2
BEC302.1	K3	3	3	3	_	3	_	_	2	2	**3**	_	2	3	**3**
BEC302.2	K3	3	3	3	**2**	3	_	_	2	2	**3**	_	2	3	**3**
BEC302.3	K3	3	3	3	_	3	_	_	2	2	**3**	_	2	3	**3**
BEC302.4	K3	3	3	3	_	3	_	_	2	2	**3**	_	2	3	**3**
BEC302.5	K3	3	3	3	**2**	3	_	_	2	2	**3**	_	2	3	**3**
BEC302 (After CBS)		**3**	**3**	**3**	**2**	**3**	_	_	**2**	**2**	**3**	_	**2**	**3**	**3**

CO PO mapping for the events conducted after gap identification

Sl. No.	Gap Identification	Activity Planned to fill the gap	CO	Relevant PO Mapping
1	PO4,PO6, PO7, PO8, PO9,PO11	Code Debugging	CO1, CO2, CO3, CO4, CO5	PO4, PO10, PSO2

CO-PO MAPPING Justification Table

Sl No.	CO	PO	Number Of Key Elements of PO Mapped To CO	Justification
CO1: Construct the truth table for the given statement and obtain the simplified logical expression				
1.	**CO1**	1	**The students will be able to gain** • Knowledge of Mathematics • Knowledge in Specific Engg. Problem & To Find Solution	3 Keywords Are Mapped Hence Strength Is 3
2.		2	**The students will be able to** • Identify • Formulate • Analyse the Problems	3
3		3	**The students will be able to gain** • **Design** system components or processes **Design** solutions for problems	3
4		5	**The students will be able to** • Design solution for complex activities • Apply appropriate techniques Use modern tools	3
5		8	**The students will be able to** Follow ethical practices in the lab	2
6		9	**The students will be able to work effectively in multidisciplinary as** • Individual In a Team	2
7		10	**The students will be able to** • Communicate through documentation	3
8		12	**The students will be able to engage in knowledge up gradation through** • Independent learning • Lifelong learning	2
9		PSO1	**The students will be able to understand the fundamentals of Electronics & Communication Engineering which can be used in** • Embedded system • Semiconductor Technology	3

10		PSO2	**The students will have the ability to** • Design a tool for societal concern • Develop solutions for hardware/software tools	3
CO2: Identify the basics of Verilog operators and data types and write the programs using data flow description				
11	**CO2**	1	**The students will be able to gain the** • Knowledge Of Mathematics • Knowledge Of Science, • Knowledge In Specific Engg. Problem & To Find Solution	3
12		2	**The students will be able to** • Identify • Formulate • Analyse Complex Engineering Problems	3
13		3	**The students will be able to gain** • **Design** system components or processes **Design** solutions for problems	3
14		4	**The students will be able to** • Analysis and interpret the data	2
15		5	**The students will be able to** • Design solution for complex activities • Apply appropriate techniques Use modern tools	3
16		8	**The students will be able to** Follow ethical practices in the lab	2
17		9	**The students will be able to work effectively in multidisciplinary as** • Individual In a Team	2
18		10	**The students will be able to** • Design documentation • Make effective presentation	3
19		12	**The students will be able to engage in knowledge upgradation through** • Independent learning Lifelong learning	2
20		PSO1	**The students will be able to gain the knowledge in the fundamentals of ECE in** • Signal Processing • Embedded systems • Communication • Semiconductor Technology	3
21		PSO2	**The students will have the ability to** • Design a tool for societal concern • Develop solutions for hardware/software tools	3
CO3: Apply the concepts of combinational logical circuits to design the digital circuits and build using MSI Components and PLD'S.				

22	CO3	1	**The students will be able to gain the** • Knowledge Of Mathematics • Knowledge Of Science, • Knowledge In Specific Engg. Problem & To Find Solution	3
23		2	**The students will be able to** • Identify • Formulate • Analyse Complex Engineering Problems	3
24		3	**The students will be able to gain** • **Design** system components or processes • **Design** solutions for problems	3
25		5	**The students will be able to** • Design solution for complex activities • Apply appropriate techniques Use modern tools	3
26		8	**The students will be able to** Follow ethical practices in the lab	2
27		9	**The students will be able to work effectively in multidisciplinary as** • Individual In a Team	2
28		10	**The students will be able to** • Communicate Effectively on complex Engg activities • Design documentation	3
29		12	**The students will be able to engage in knowledge upgradation through** • Independent learning Lifelong learning	2
30		PSO1	**The students will be able to gain the fundamentals of ECE in** • Embedded systems • Semiconductor Technology	3
31		PSO2	**The students will be able to gain the ability to** • Design a tool for societal concern	3
CO4: Make use of flip flops to build the sequential circuits.				
32	CO4	1	**The students will be able to gain the** • Knowledge Of Mathematics • Knowledge Of Science, • Knowledge In Specific Engg. Problem & To Find Solution	3
33		2	**The students will be able to** • Identify • Formulate • Analyse Complex Engineering Problems	3
34		3	**The students will be able to** • **Design** solutions for public health & safety • **Design** solutions for environmental considerations	3

35		5	**The students will be able to** • Design solution for complex activities • Apply appropriate techniques Use modern tools	3
36		8	**The students will be able to** Follow ethical practices in the lab	2
37		9	**The students will be able to work effectively in multidisciplinary as** • Individual In a Team	2
38		10	**The students will be able to** • Communicate Effectively on complex Engg activities • Design documentation	3
39		12	**The students will gain the ability to engage in knowledge upgradation through** • Independent learning • Lifelong learning	2
40		PSO1	**The students will be able to gain the knowledge in the fundamentals of ECE in** • Signal Processing • Embedded systems • Communication • Semiconductor Technology	3
41		PSO2	**The students will be able to gain the ability to** • Design a tool for societal concern • Develop solutions for hardware/software tools	3
CO5: Apply the concepts of behavioral and structural descriptions to develop Verilog programs for digital circuits.				
42	**CO5**	1	**The students will be able to gain** • Knowledge 0f Mathematics • Knowledge n Specific Engg. Problem • To find solution for the problems	3 Keywords Are Mapped Hence Strength Is 3
43		2	**The students will be able to** • Identify • Formulate • Analyse Complex Engineering Problems	3
44		3	**The students will be able to** • **Design** solutions for public health & safety • **Design** solutions for environmental considerations	3
45		4	**The students will be able to** • **Design the experiments** • **Analysis and interpret the data**	2
46		5	**The students will be able to** • Design solution for complex activities • Apply appropriate techniques Use modern tools	3

47		8	**The students will be able to** Follow ethical practices in the lab	2
48		9	**The students will be able to work effectively in multidisciplinary as** • Individual In a Team	2
49		10	**The students will be able to** • Communicate Effectively on complex Engg activities • Design documentation	3
50		12	**The students will have the ability to engage in knowledge upgradation through** • Independent learning • Lifelong learning	2
51		PSO1	**The students will be able to gain the knowledge in the fundamentals of ECE in** • Signal Processing • Embedded systems • Communication • Semiconductor Technology	3
52		PSO2	**The students will be able to gain the ability to** • Design a tool for societal concern • Develop solutions for hardware/software tools	3

Signature of Course In-charge **Signature of Module Coordinator** **Signature of HOD-ECE**

KS INSTITUTE OF TECHNOLOGY BANGALORE

DEPARTMENT OF ELECRONICS & COMMUNICATION ENGINEERING

NAME OF THE COURSE INCHARGE : Bhargavi Ananth

COURSE CODE/NAME :BEC302/DIGITAL SYSTEM DESIGN USING VERILOG

SEMESTER/YEAR/SEC :III/ II/B

ACADEMIC YEAR :2023-24

Sl. No.	Topic to be covered	Mode of Delivery	Teaching Aid	No. of Periods	Cumulative No. of Periods	Proposed Date (B)
1	Introduction to combinational logic. Definition of combinational logic	L	BB	1	1	22/11/23
2	Introduction to combinational logic. Definition of combinational logic	L	BB	1	2	22311/23
3	Canonical forms	L	BB	1	3	25/11/23
4	Canonical forms	L	BB	1	4	27/11/23
5	Generation of switching equations from truth tables	L	BB	1	5	28/11/23
6	Generation of switching equations from truth tables	L	BB	1	6	29/11/23
7	Karnaugh maps- up to 4 variables	L	BB	1	7	4/12/23
8	Quine-McCluskey Minimization Technique	L	BB	1	8	5/12/23
9	Quine-McCluskey using Don't Care Terms	L	BB	1	9	6/12/23
MODULE 4: Introduction to Verilog						
10	Structure of Verilog module	L	BB	1	10	7/12/23

11	Operators, Data Types	L	BB	1	11	9/12/23
12	Styles of Description	L	BB	1	12	11/12/23
13	Verilog Data flow description	L	BB	1	13	12/12/23
14	Highlights of Data flow description	L	BB	1	14	13/12/23
15	Highlights of Data flow description	L	BB	1	15	14/12/23
16	Highlights of Data flow description	L	BB	1	16	18/12/23
17	Structure of Data flow description	L	BB	1	17	19/12/23
18	Structure of Data flow description	L	BB	1	18	20/12/23
MODULE 2: Logic Design with MSI Components and Programmable Logic Devices						
19	Binary Adders and Subtractors	L	BB	1	19	21/12/23
20	Comparators	L	BB	1	20	23/12/23
21	Decoders	L	BB	1	21	26/12/23
22	Decoders	L	BB	1	22	27/12/23
23	Encoders, Multiplexers,	L	BB	1	23	28/12/23
24	Encoders, Multiplexers,	L	BB	1	24	30/12/23
25	Programmable Logic Devices (PLDs)	L	BB	1	25	4/1/24
26	Programmable Logic Devices (PLDs)	L	BB	1	26	8/1/24
27	Revision	L	BB	1	27	9/1/24
MODULE 3: Flip-Flops and its Applications						
28	The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops,	L	BB	1	28	10/1/24
29	Characteristic equations	L	BB	1	29	11/1/24
30	Registers	L	BB	1	30	13/1/24
31	Binary Ripple Counters	L	BB	1	31	16/1/24
32	Synchronous Binary Counters	L	BB	1	32	17/1/24
33	Synchronous Binary Counters	L	BB	1	33	18/1/24
34	Counters based on Shift Registers	L	BB	1	34	22/1/24
35	Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops.	L	BB	1	35	23/1/24
36	Design of Synchronous mod-n Counter	L	BB	1	36	24/1/24

	using clocked T, JK, D and SR flip-flops.					
MODULE 5: Verilog Behavioral description						
37	Structure	L	BB	1	37	25/1/24
38	Variable Assignment Statement	L	BB	1	38	27/1/24
39	Sequential Statements, Loop Statements	L	BB	1	39	29/1/24
40	Verilog Behavioral Description of Multiplexers	L	BB	1	40	30/1/24
41	Verilog Structural description	L	BB	1	41	31/1/24
42	Highlights of Structural description	L	BB	1	42	1/2/24
43	Organization of structural description	L	BB	1	43	5/2/24
44	Structural description of ripple carry adder	L	BB	1	44	6/2/24
45	Revision	L	BB	1	45	7/2/24

Signature of Course Incharge **Signature of Module Coordinator** **Signature of HOD**

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-560109DEPARTMENT OF ELECTRONICS &COMMUNICATION ENGG

ACADEMIC YEAR : 2022-2023

FIRST ASSIGNMENT QUESTIONS

Academic Year	**2022-23**		
Batch	**2021-2025**		
Semester / Section	**3/A & B**		
Course Code-Title	**Digital system design using Verilog BEC302**		
Name of the Instructor	**Mrs. BHARGAVI ANANTH** **Mr. NAVEEN KUMAR S**	**Dept**	**ECE**

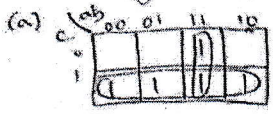
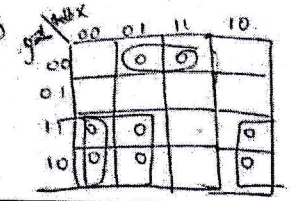
Assignment No: 1 **Total marks:10**
Date of Issue: 12/12/23 **Date of Submission: 19/12/23**

Sl.No	Assignment Questions	K Level	CO	Marks
1.	**Solve** the following using K Map Y=f(a,b,c)= ∑m(1,3,5,6,7) Y=f(w,x,y,z)= πM(2,3,4,6,7,10,11,12)	K3 Applying	CO1	2
2	**Solve** the following using Quine McClusky Technique R= f(a,b,c,d)= ∑m(2,3,4,5,13,15) + ∑md(8,9,10,11)	K3 Applying	CO1	2
3	**Explain** Structure of Verilog Module and Verilog ports	K2 Understanding	CO2	2
4	**Make use of** Data Flow Description to write the Verilog code for the following expression Y= (A+B).C'D Y=AB+CD'	K3 Applying	CO2	2
5	**Construct** the Circuit of 4 bit Carry Lookahead adder	K3 Applying	CO3	2

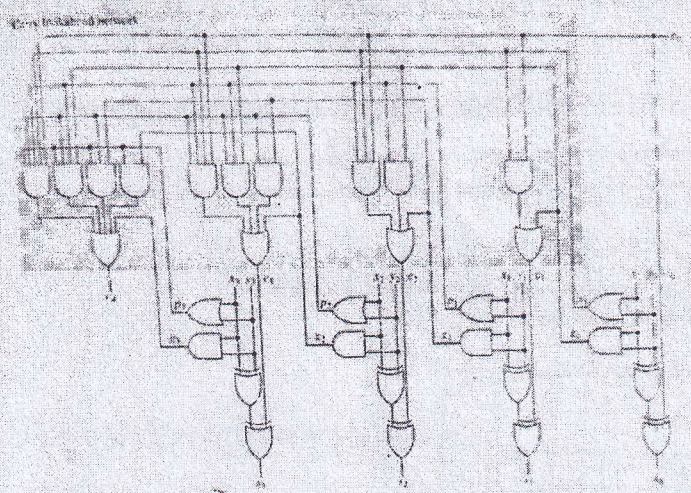
Faculty in charge Module Coordinator HOD

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
2023 – 24 EVEN SEMESTER

SCHEME AND SOLUTION OF ASSIGNMENT 1

Q.NO.	POINTS	MARKS
1	Solve using K map (a)  $y = f(a,b,c) = ab + c$ (b)  $y = \pi (x'+y+z)(w+y')(x+y')$	2
2	Grp 1 Minterm: (2,3), (2,10), (4,5), (8*,9*), (8*,10), (3,11), (5,13) a b c d: 0 0 1 -; - 0 1 0; 0 1 0 -; 1 0 0 -; 1 0 - 0; - 0 1 1; - 1 0 1 eqn. = $b'c + ad$	2
3	Structure of Verilog – Body, Declaration Ports – input, output, inout	2

4	module exp1(input A, B, C, D,
	output y);
	assign y = (A&B) | (C&(~D));
	endmodule
	module exp2(input A, B, C, D,
	output y);
	assign y = (A|B) & ((~C)&D);
	endmodule
		2

5		2

$g_i = x_i y_i \qquad p_i = x_i + y_i$

$c_{i+1} = g_i + p_i c_i$

$c_1 = g_0 + p_0 c_0 \qquad c_2 = g_1 + p_1 c_1$

$= g_1 + p_1 g_0 + p_1 p_0 c_0$

$c_3 = g_2 + p_2 c_2 = g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0$

Course in charge

Module Coordinator

HOD

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-560109

DEPARTMENT OF ELECTRONICS &COMMUNICATION ENGG

ACADEMIC YEAR : 2022-2023

SECOND ASSIGNMENT QUESTIONS

Academic Year	2022-23		
Batch	2021-2025		
Semester / Section	3/A & B		
Course Code-Title	Digital system design using Verilog BEC302		
Name of the Instructor	Mrs. BHARGAVI ANANTH Mr. NAVEEN KUMAR S	Dept	ECE

Assignment No: 2 **Total marks:10**

Date of Issue: 20/1/24 **Date of Submission:** 28/1/24

Sl.No	Assignment Questions	K Level	CO	Marks
1.	Design Mod-6 Counter for the sequence 0,2,3,6,5,1 using T flipflop	K3 Applying	CO3	2
2	Explain structure of data flow description with example	K3 Applying	CO4	2
3	Explain different types of Datatypes present in Verilog with an example	K3 Understanding	CO4	2
4	Explain the Structure of Verilog Behavioral description with an example	K3 Applying	CO5	2
5	Construct (Write) a Verilog code for 2:1 MUX using ELSE IF statement.	K3 Applying	CO5	2

Naveen Kumar S
Faculty in charge

Module Coordinator

HOD

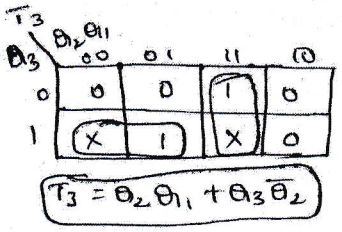
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
2023 – 24 EVEN SEMESTER

SCHEME AND SOLUTION OF ASSIGNMENT 2

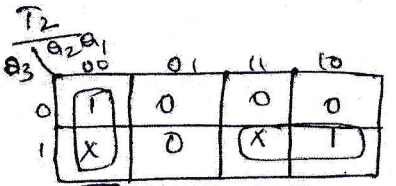
Q.NO. 1 — MARKS: 2

Excitation table for mod-6 Counter using T-flip flop

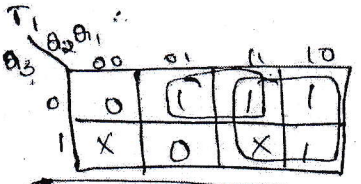
Present State $Q_3\ Q_2\ Q_1$	Next state $Q_3^+\ Q_2^+\ Q_1^+$	Inputs to FF $T_3\ T_2\ T_1$
0 0 0	0 1 0	0 1 0
0 1 0	0 1 1	0 0 1
0 1 1	1 1 0	1 0 1
1 1 0	1 0 1	0 1 1
1 0 1	0 0 1	1 0 0
0 0 1	0 0 0	0 0 1



$T_3 = Q_2Q_1 + Q_3\overline{Q_2}$



$\overline{T_2} = \overline{Q_2}\overline{Q_1} + Q_3Q_2$



$T_1 = Q_2 + \overline{Q_3}Q_1$

Realization using the above equations

2 — MARKS: 2

Structure of data-flow description
- Body, declaration, Ports - input, output, inout

Example Program

3

Nets:

These are declared by the predefined word **"wire"**. Nets values are change continuously by the circuits that are driving them. A wire represents a physical wire in a circuit and is used to connect gates or modules. The value of a wire can be read, but not assigned to, in a function or block. Verilog supports 4 values for nets.

Value	Net Definition	Reg
0	Logic 0(false)	Logic 0
1	Logic 1(true)	Logic 1
X	Unknown	Unknown
Z	High impedance	High impedance

Eg. Wire sum; // statement declares a net by name sum.

Wire s1=1'b0; // this statement declares a net by the name of s1; it is initial value 1 bit with value 0.

Registers: Registers store values until they are updated. They are data storage elements. Declared by the predefined word **"reg"** Verilog supports 4 values for registers. As shown in above table.

Eg reg sum_total; // declares a register by the name sum_total.

Vectors:

These are multiple bits. A reg or net can be declared as a vector. Vectors are declared by brackets [].

Eg. Wire [3:0] a=4'b1010;

Reg [7:0] total=8'd12;

Integer: declared by the predefined word **"integer"**. Integers are general-purpose variables. For synthesis they are used mainly loops-indices, parameters, and constants.

Eg. Integer no_bits;//The above statement declares no_bits as an integer.

Real:

Real (floating point) numbers are declared with the predefined word **"real"**. Examples of real values are 2.4, 56.3 5e12.

Eg. Real weight; // the statement declares the register weight as real.

2

4	**Verilog description**
	`module halfadd(a, b, sum, carry);`
	`input a, b;`
	`output sum, carry;`
	`reg sum, carry;` /*since sum and carry are outputs and they are written inside "always", they should be declared as "reg" or else it will result in syntax error/*
	`always @(a, b)`
	`begin`
	`#10 sum = a^b;` //statement1-procedural as it is inside always.
	`#10 carry = a&b;` //statement2- procedural as it is inside always.
	`end`
	`endmodule`
	In the above example
	*The name of the module is halfadd. It has two inputs a and b, two outputs sum and carry.
	*Any signal declared as output should be declared as a register (reg).Therefore sum and carry are declared as registers.
		2

5	Verilog 2x1 Multiplexer Using ELSE-IF
	`module MUXBH (A, B, SEL, Gbar, Y);`
	`input A, B, SEL, Gbar;`
	`output Y;`
	`reg Y;`
	`always @ (SEL, A, B, Gbar)`
	`begin`
	`if (Gbar == 0 & SEL == 1)`
	`begin`
	`Y = B;`
	`end`
	`else if (Gbar == 0 & SEL == 0))`
	`Y =A;`
	`else`
	`Y = 1'bz;`
	`end`
	`endmodule`
		2

Course in charge

Module Coordinator

HOD

ASSIGNMENT - 3

CODE DEBUGGING

Each student has to correct the errors in five of the erroneous programs given below. They have to prepare a report of the same mentioning the error programs and the corrected programs.

PROGRAMS WITH ERRORS

1. LOGIC GATES

```
module LogicGates(a,b,y1,y2,y3,y4,y5,y6,y7)
input a,b;
output y1,y2,y3,y4,y5,y6,y7;
and(y1,a,b);
or(y2,a,b);
not(y3,a);
n_and(y4,a,b);
nor(y5,a,b);
xor(y6,a,b);
xnor(y7,a,b);
end module;
```

2. HALF ADDER

```
module Half Adder(a,b,sum,carry);
input a,b;
output sum,carry;
sum = a ^b;
carry = a&b
endmodule
```

3. CARRY LOOKAHEAD ADDER

```
module CLA_Adder(a,b,cin,sum,cout);
input[3:0] a,b;
input cin;
output 3:0 sum;
output cout;
assign p0=(a[0]^b[0]),
p1=(a[1]^b[1]),
p2=(a[2]^b[2]),
p3=(a[3]^b[3]);
assign g0==(a[0]&b[0]),
```

```
g1=(a[1]&b[1]),
g2=(a[2]&b[2]),
g3=(a[3]&b[3]);
assign c0=cin,
c1=g0|(p0&cin),
c2=g1|(p1&g0)|(p1&p0&cin),
c3=g2|(p2&g1)|(p2&p1&g0)|(p1&p1&p0&cin)
c4=g3|(p3&g2)|(p3&p2&g1)|(p3&p2&p1&g0)|(p3&p2&p1&p0&cin);
assign sum[0]=p0^c0,
sum[1]=p1^c1,
sum[2]=p2^c2,
sum[3]=p3^c3;
assign cout=c4

end module
```

4. 8:3 ENCODER

```
module Encoder(d0,d1,d2,d3,d4,d5,d6,d7,a,c);
input d0,d1,d2,d3,d4,d5,d6,d7;
output a,c;
or(a,d4,d5d6,d7);
or(b,d2,d3,d6,d7);
dor(c,d1,d3,d5,d7);
endmodule;
```

5. 8:1 MULTIPLEXER

```
mod Mulitplexer(d0,d1,d2,d3,d4,d5,d6,d7,sel,out);
input d0,d1,d2,d3,d4,d5,d6,d7;
input [2:0] sel;
output reg out;
always@(sel);
begin
case(sel)
3'000:out=d0;
3'001:out=d1;
3'010:out=d2;
3'011:out=d3;
3'100:out=d4;
3'101:out=d5;
3'110:out=d6;
3'111:out=d7;
endcase
end
endmodule
```

6. FULL ADDER

```
module FullAdder(A,B,Cin,Sum,Cout)
input [3:0]A,B;
input Cin;
output [3:0]Sum;
output cout;
wire [3:0]temp;
assign temp=A+B+Cin;
assign Sum=temp[3:0];
assign Cout=temp[4];
endmodule
```

7. COMPARATOR

```
module Comparator(A,B,gt,lt,eq);
 [3:0] A,B;
output reg gt,lt,eq;

always @(A,B)

if(A>B)
begin
gt=1;
eq=0;
lt=0;
end
else if(A < B);
begin
gt=0;
eq=0;
lt=1;
end
else
begin
gt=0;
eq=1;
lt=0;
end
end
endmodule
```

8. HALF SUBTRACTOR

```
module HalfSubstractor(a,b,difference,borrow);
input a,b;
output difference,borrow;
xor(a,b,difference);
assign borrow=(~A&b);
endmodule
```

9. D FLIP FLOP

```
module D_Flipflop(Din,clk,reset,q);
input Din,clk,reset;
output q;
always@(posedgeclk)
begin
if(reset)
q=1'b0;
else
q=Din
end
endmodule
```

10. SHIFT REGISTER

```
module ShiftRegister_SIPO(C, SI, PO);
input C,SI
output [7:0] PO;
reg [7:0] tmp;

always @(posedge C)
begin
tmp = {tmp[6:0], SI};

assign PO = tmp;

end
endmodule
```

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
FIRST INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET: A

USN										

Degree : B.E
Branch – Stream : ECE
Course Title : Digital System Design using Verilog
Duration : 1 ½ Hr (90 minutes)

Semester : III
Course Type / Code : BEC302
Date : 2/1/2024
Max Marks : 50

Note: Answer **ONE full** question from each module

K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 1			
a)	**Solve** the following (i) Convert the following Boolean function into minterm canonical or maxterm canonical form: $f(w,x,y,z) = \bar{w}z + y\bar{z}$ (ii) $y = (A + \bar{B} + C)(\bar{A} + D)$ (ii) $f(A,B,C,D) = \Sigma m(1,2,3,5,6,7,9,10,11)$ using K Map and obtain the minimized SOP and POS expressions	20 (12+8)	CO1	K3
(b)	**Make use of** Quine Mc Cluskey Method to simplify the given boolean function $f(a,b,c,d) = \Sigma m(0,1,2,3,6,7,8,9,14,15)$		CO1	K3
	OR			
2(a)	**Make use of** QM technique to simplify the function $f(A,B,C,D) = \Sigma m(9,12,13,15) + \Sigma d(1,4,5,7,8,11,14)$. **Identify** the essential prime implicants if any and obtain atleast two solutions.	20 (12+8)	CO1	K3
(b)	Four chairs A,B,C,D are placed in a row. Each chair may be occupied (logic 1) or not occupied (logic 0). The output Y should go high only when adjacent chairs are occupied. Draw the truth table, **Solve** for the maxterm expression and simplify the expression using K Map to get minimum POS expression. Draw the logic diagram to realize this expression using gates.		CO1	K3
	Module 2			
3(a)	**Explain** the structure of Dataflow description with an example.**Construct** a Verilog Code for full subtractor in DataFlow style and draw the truth table and simplified equations and logic diagram.	20 (12+8)	CO2	K3
(b)	Discuss Assigning a delay time to signal Assignment statement by taking an example of half adder. Assume each gate has a delay of 6 ns. **Develop** the logic diagram, logic circuit, truth table, program and waveform.		CO2	K3
	OR			
4(a)	**Construct** a Verilog code for half subtractor using Dataflow, Behavioral and structural and explain them.	20(12+8)	CO2	K3
(b)	**Explain** logical, shift and comparison operators in Verilog.		CO2	K2
	Module 3			
5	**Model** a parallel ripple adder using binary full adder. Draw the truth table and logic diagram for binary adder, simplify the expression for sum and carry. Draw the block diagram for ripple parallel adder. Why is it called as ripple parallel adder?	10	CO3	K3
	OR			
6	**Make use of** a Truth table to compare BCD and binary sums and obtain the simplified expression for cout and hence obtain simplified block diagram of the same.	10	CO3	K3

Name & Signature of Course In charge

Name & Signature of Module Coordinator

HOD

Principal

Selected

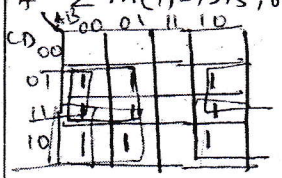
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

SECOND INTERNAL TEST QUESTION PAPER 2023 – 24 ODD SEMESTER

SCHEME AND SOLUTION (SET A)

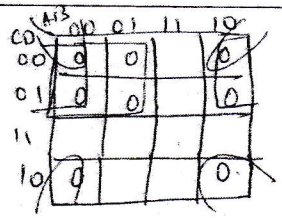
Degree : B.E
Branch : ECE
Course Title : Digital System Design using Verilog

Semester : III A &B
Course Code : BEC302
Max Marks : 50

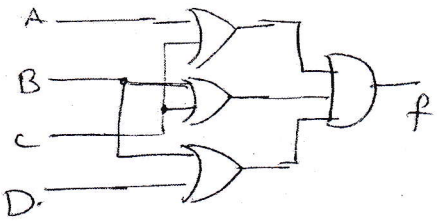
Q.NO.	POINTS	MARKS
1(a)	(i) $f = \bar{w}z + y\bar{z} = \bar{w}xz + \bar{w}\bar{x}z + \bar{w}y\bar{z} + \bar{w}y\bar{z}$ $= \bar{w}xyz + \bar{w}x\bar{y}z + \bar{w}\bar{x}yz + \bar{w}\bar{x}\bar{y}z +$ $\bar{w}xy\bar{z} + \bar{w}\bar{x}y\bar{z} + wxy\bar{z} + w\bar{x}y\bar{z}$	3M
	(ii) $y = (A+\bar{B}+C)(\bar{A}+D)$ $= (A+\bar{B}+C+D)(A+\bar{B}+C+\bar{D})(\bar{A}+B+D)$ $(\bar{A}+\bar{B}+D)$ $= (A+\bar{B}+C+D)(A+\bar{B}+C+\bar{D})(\bar{A}+B+C+D)$ $(\bar{A}+B+\bar{C}+D)(\bar{A}+\bar{B}+C+D)(\bar{A}+\bar{B}+\bar{C}+D)$	3M
	(i) $f = \sum m(1,2,3,5,6,7,9,10,11)$	
	(ii)  $f = \bar{A}D + \bar{B}D + \bar{B}C + \bar{A}C$ $f = (C+D)(\bar{A}+\bar{B})$	3+3
1(b)	a b c d 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 8 1 0 0 0 3 0 0 1 1 6 0 1 1 0 9 1 0 0 1 7 0 1 1 1 14 1 1 1 0 15 1 1 1 1 0,1 0 00 ✓ 7,15 – 111 ✓ 0,2 0 0 0 ✓ 14,15 111 – ✓ 0,8 – 0 0 0 ✓ 0,1,2,3 0 0 – – 1,3 0 0 – 1 ✓ 0,8,1,9 – 0 0 – 1,9 – 0 0 1 ✓ 2,6,3,7 0 – 1 – 2,3 0 0 1 – ✓ 6,7,14,15 – 1 1 – 2,6 0 – 1 0 ✓ 8,9 1 0 0 – ✓ 3,7 0 – 1 – 1 ✓ 6,7 0 1 1 – ✓ 6,14 – 1 1 0 ✓ $f = b'c' + bc + a'b'$ on $b'c' + bc + a'c$ 0 1 2 3 6 7 8 9 14 15 $a'b'$ × × × × $b'c'$ × × $a'c$ × × × × bc × ×	2+2+2 +2

2(a) (3+3+2)

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



$f = (A+C)(B+C)(B+D)$



2(b) 2+3+3+3+1

A	B	C	D
1* 0	0	0	1
4* 0	1	0	0
8* 1	0	0	0
5* 0	1	0	1
9 1	0	0	1
12 1	1	0	0
7* 0	1	1	1
11* 1	0	1	1
13 1	1	0	1
14* 1	1	1	0
15 1	1	1	1

1*,5* 0-01 ✓
1,9 -001 ✓
4*,5* 010- ✓
4*,12 -100 ✓
8*,9 100- ✓
5*,7* 01-1
5*,13 -101 ✓
9,11* 10-1 ✓
9,13 1-01 ✓
12,13 110- ✓
12,14 11-0 ✓
7*,15 -111

11*,15 1-11 ✓
13,15 11-1 ✓
14*,15 111- ✓

1*,5*,9,13 --01
5*,15*,12,13 10--
8*,9,12,13 1--0
9,11*,13,15 1--1
12,14,13,15 11--
5*,13,7*,15 -1-1

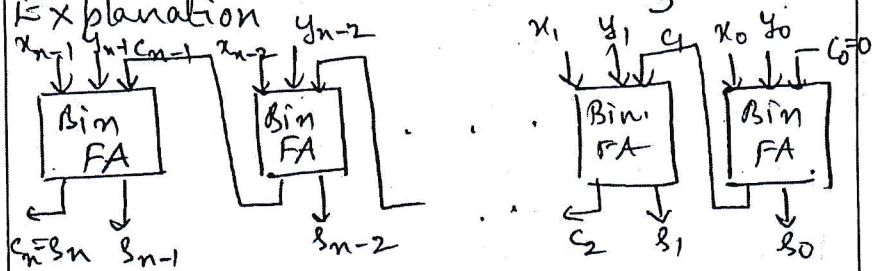
	1*	4*	5*	7*	8*	9	11*	12	13	14*	15
c'd	×		×			×			×		
bc'		×	×					×	×		
ac'						×	×		×		×
ad						×	×	●	×	●	×
ab								×	×	×	×
bd			×	×					×		×

Solutions

c'd + ad + b*c' or c'd + ad + ab

3(a)	Dataflow defn. — 1 Structure — 2 Concurrent — 1 example. — 2	6
3(b)	~~Assignment~~ signal declaration and assignment — 1 logic dgm — 1 logic ckt — 1 TT — 1 program — 2 W/f — 2 sum ~~diff~~ = $a \oplus b$ cout ~~bor~~ = $\bar{a}b$	8
3(c)	Code — 3 Eqns sum = $a \oplus b \oplus c$ carry = $ab + bc + ac$ } 1 TT — 1, logic dgm — 1	6
4(a)	Verilog code Dataflow — 2 + 1 (explain) Behavioral — 3 + 2 (sequential) Structural — 3 + 2 (explain) diff = $a \oplus b$ br = $\bar{a}b$.	12
4(b)	~~Logical~~ ~~Arithmetic~~ → *, |, ^, ~, &&, ||, unary & ~~+, -, /, *, %~~ & ~~!~~ Shift → >> << Comparison → >, <, >=, <=, ==, != === !==	3 2 3

5) TT of Full adder – 1
Simplification – 2 $sum = a \oplus b \oplus c$
and expressions $c_{i+1} = ab + bc + ac$
logic dgm – 2.
Parallel ripple binary adder block dgm – 2
Explanation – 3



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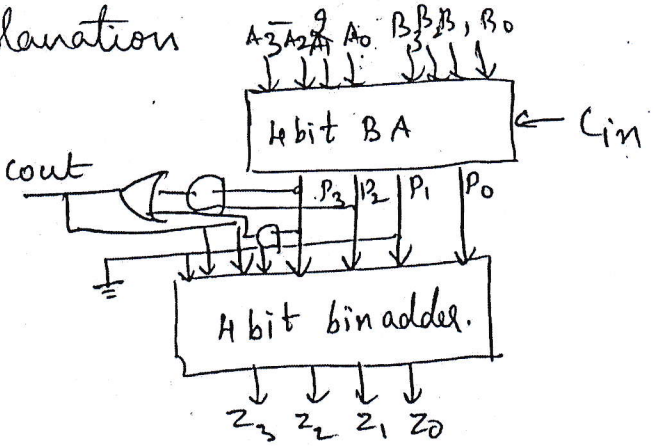
6) Binary & BCD sum TT – 3.
Simplification – 2.
Single decade BCD adder block dgm – 3
Explanation



10

Course in charge
Module Coordinator
HOD

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
FIRST INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET:B

USN										

Degree : **B.E** | **Semester** : **III**
Branch - Stream : **ECE** | **Course Type / Code** : **BEC302**
Course Title : **DSDV** | **Date** : **02/01/2024**
Duration : **1 ½ Hr (90 minutes)** | **Max Marks** : **50**

Note: Answer **ONE full** question from each module
K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 1			
1(a)	Define Combinational Logic circuit. **Construct** the truth table for a combinational logic circuit that has 4 inputs and the output will high when the majority of the inputs are high.	20 (4+6+ 10)	CO1	K2
(b)	**Apply** the concept of minterm and maxterm to convert the following Boolean function into minterm canonical or maxterm canonical form: **1)**f (A, B, C) =$\bar{A}$B+$\bar{B}$C (SOP) **2)** f (A, B, C) =A+AB+ABC (SOP) **3)**f (A, B, C) =(A+B) (B+C) (A+C) (POS)		CO1	K3
(c)	**Construct** the truth table and obtain the expressions for binary to Excess 3 then simplify the output expressions using Kmap		CO1	K3
	OR			
2(a)	**Explain** the following with example .1) Literal 2) Minterm 3) Maxterm 4) Canonical SOP 5) Canonical POS	20(5+ 5+10)	CO1	K2
(b)	**Solve** the below expressions **1)**Y=f(A, B,C)= ∑(0,1,3,5) **2)**Y=∑(0,1,5,9,13,14,15)+ ∑d(3,4,7,10,11) using K Map and obtain the minimized SOP and POS expressions		CO1	K3
(c)	**Make use of** Quine Mc Cluskey Method to simplify the given Boolean function S= f (A, B, C, D) = ∑ M(0,1,3,7,8,9,11,15)		CO1	K3
	Module 2			
3(a)	What is HDL. **Explain** the structure of Verilog module with an example	20(5+ 6+9)	CO2	K2
(b)	**Explain** Verilog Arithmetic and Logical operators with example.		CO2	K2
(c)	**Compare** different types /styles of Verilog descriptions with example of half adder.		CO2	K2
	OR			
4(a)	List out the different types of Data types present in Verilog and **explain** its working with an example	20(6+ 5+9)	CO2	K2
(b)	**Explain** Signal declaration and Assignment statements with example		CO2	K2
(c)	Discuss Assigning a delay time to signal Assignment statement by taking an example of 2x1 Mux with active low enable. **Draw** the logic diagram, logic circuit, truth table, program, and waveform.		CO2	K2
	Module 3			
5	**Construct** and explain a parallel ripple binary subtracter using parallel binary adder. Draw the truth table and logic diagram for binary subtracter, simplify the expression for difference and borrow. Draw the block diagram for Parallel binary adder/subtracter.	10	CO3	K3
	OR			
6	**Construct** a general organization and sigma block of carry Lookahead adder with necessary equations and explain how ripple effect is eliminated.	10	CO3	K3

Name & Signature of Course In charge: | **Name & Signature of Module Coordinator:** | **HOD** | **Principal**

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

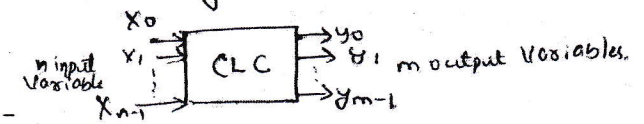
SECOND INTERNAL TEST QUESTION PAPER 2023 – 24 ODD SEMESTER

SCHEME AND SOLUTION (SET B)

Degree : B.E
Branch : ECE
Course Title : Digital System Design using Verilog

Semester : III A &B
Course Code : BEC302
Max Marks : 50

Q.NO.	POINTS	MARKS
1 a)	Logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved the resulting circuit is called Combinational logic CKt. (1)	4



(1)

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(2)

b) ① $f(A,B,C) = \bar{A}B + \bar{B}C$

$= \bar{A}B(C+\bar{C}) + \bar{B}C(A+\bar{A})$

$= \bar{A}BC + \bar{A}B\bar{C} + \bar{B}CA + \bar{B}C\bar{A}$

$= \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C} + \bar{A}\bar{B}C$ (2)

② $f(A,B,C) = A + AB + ABC$

$= A(B+\bar{B})(C+\bar{C}) + AB(C+\bar{C}) + ABC$

$= (AB + A\bar{B})(C+\bar{C}) + ABC + AB\bar{C} + ABC$ (2)

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + AB\bar{C} + ABC$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$

(B) $f(A,B,C) = (A+B)(B+C)(A+C)$

$= (A+B)+(C\bar{C})\ (B+C)+(A\bar{A})\ (A+C)+(B\bar{B})$

$= (A+B+C)(A+B+\bar{C})\ (B+C+A)\ (B+C+\bar{A})$ (2)

$(A+C+B)\ (A+C+\bar{B})$

$= (A+B+C)\ (A+B+\bar{C})\ (\bar{A}+B+C)\ (A+\bar{B}+C)$

6

(C) Truth table

Binary W X Y Z	Excess-3 A B C D
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
⋮	⋮
1 0 0 1	1 1 0 0
1010 - 1111	don't care.

(4)

10

Expression for A, B, C and D is

$A = \sum(5,6,7,8,9) + \sum d(10,11,12,13,14,15)$

$B = \sum(1,2,3,4,9) + \sum d(10,11,12,13,14,15)$

$C = \sum(0,3,4,7,8) + \sum d(10,11,12,13,14,15)$

$D = \sum(0,2,4,6,8) + \sum d(10,11,12,13,14,15)$

(2)

K-map for A and simplified expression (1)
K-map for B and simplified expression (1)
K-map for C and simplified expression (1)
K-map for D and simplified expression (1)

2) (Q) (1) Literal:- Each occurrence of a variable is called literal. (1)
Ex:- A, B, etc

(2) Minterm:- Each individual term in standard SOP form is called minterm (1)
ABC, $A\bar{B}C$

(3) Maxterm:- Each individual term in standard POS form is called maxterm (1)
$(A+B+C)$ $(\bar{A}+B+\bar{C})$

(4) Canonical SOP:- Each term in SOP form contains all the literals is called Canonical SOP (1)
$AB\bar{C} + ABC + \bar{A}B\bar{C}$

5

Canonical POS:- Each term in POS form contains all the literals then POS form is called Canonical POS.

$(A+\bar{B}+C)\ (\bar{A}+\bar{B}+C)$ (1)

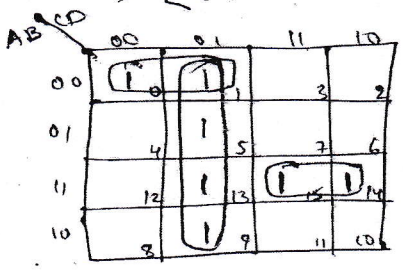
2) b) $y=(A,B,C)\sum(0,1,3,5)$

$= \bar{A}\bar{B} + \bar{A}B + \bar{A}C$ (2)

$y=(A+B)\ (A+\bar{B})\ (A+\bar{C})$

(ii) $y=A(A,B,C,D)=\sum(0,1,5,9,13,14,15)+\sum d(3,4,7,10,11)$

5



(3)

$y=\bar{C}D + \bar{A}\bar{B}\bar{C} + ABC$

$y=(C+\bar{D})\ (A+B+C)\ (\bar{A}+\bar{B}+\bar{C})$

2 c)

Min term	B.R
m_0	0000
m_1	0001
m_3	0011
m_7	0111
m_8	1000
m_9	1001
m_{11}	1011
m_{15}	1111

Min term	B.R
m_0	0000 ✓
m_1	0001 ✓
m_8	1000 ✓
m_3	0011 ✓
m_9	1001 ✓
m_7	0111 ✓
m_{11}	1011 ✓
m_{15}	1111 ✓

Min	B.R
(0,1)	000- ✓
(0,8)	-000 ✓
(1,3)	00-1 ✓
(1,9)	-001 ✓
(8,9)	100- ✓
(3,7)	0-11 ✓
(3,11)	-011 ✓
(9,11)	10-1 ✓
(7,15)	-111 ✓
(11,15)	1-11 ✓

Min	B.R	
(0,1,8,9)	-00-	(A)
(0,8,1,9)	-00-	
(1,3,9,11)	-0-1	(B)
(1,9,3,11)	-0-1	
(3,7,11,15)	--11	(C)
(3,11,7,15)	--11	

P.I chart

Prime Implicants		m_0	m_1	m_3	m_7	m_8	m_9	m_{11}	m_{15}
(0,1,8,9)	$\bar{B}\bar{C}$ -00-	(X)	X			(X)	X		
(1,3,9,11)	$\bar{B}D$ -0-1		X	X			X	X	
(3,7,11,15)	CD --11			X	(X)			X	(X)

$y=\bar{B}\bar{C}+CD$

2+2+2

2+2

= 10

3) a)	HDL defination — 1 Structure — 2 example — 3	5
b)	Arithemetic operators +, −, /, *, %, **, {, } — 3 example Logical operators &, |, ~(&), ~(|), ^, ~^, ~ — 3 example.	6.
c)	Dataflow description with example — 3 Structural description with example — 3 Behavioral description with example — 3	9.
4) a)	Verilog data types Nets, Registers, Vectors, Integers / Real, Parameters, Arrays working with example	6
b)	Logic circuit — 1 Signal declarations — 2 with explanation. Explanation of two phases — 3	6
c)	example for Assigning a delay to statement — 1 8x1 mux Truth table — 1 logic diagram & Circuit — 2 Program — 1 waveform — 1 Analysis — 3	9

⑥ **Carry Lookahead Adder**

Generation of Carry Equations

$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$

$C_{i+1} = x_i y_i + (x_i + y_i) C_i$

$g_i = x_i y_i$ Eqn ①

$P_i = x_i + y_i$ Eqn ②

$\therefore C_{i+1} = g_i + P_i C_i$

$C_1 = g_0 + P_0 C_0$ ∴ $C_2 = g_1 + P_1 C_1$ — 3

$= g_1 + P_1 (g_0 + P_0 C_0)$

$= g_1 + P_1 g_0 + P_1 P_0 C_0$

Similarly

$C_3 = g_2 + P_2 g_1 + P_2 P_1 g_0 + P_2 P_1 P_0 C_0$

$C_4 = g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0 + P_3 P_2 P_1 P_0 C_0$

$C_{i+1} = g_i + P_i g_{i-1} + P_i P_{i-1} g_{i-2} + \cdots + P_i P_{i-1} \cdots P_1 g_0 + P_i P_{i-1} \cdots P_0 C_0$

10

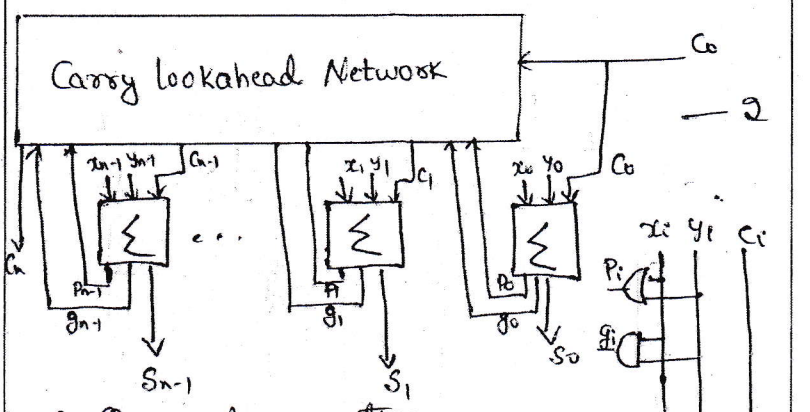


fig ⑥ General organization

fig ⑤ Sigma block

Explanation on ripple Effect is eliminated — ④

Naveen Kumar S
Course in charge

Module Coordinator

HOD

⑥ **Carry Lookahead Adder**

Generation of Carry Equations

$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$

$C_{i+1} = x_i y_i + (x_i + y_i) C_i$

$g_i = x_i y_i$ Eqn ①

$P_i = x_i + y_i$ Eqn ②

$\therefore C_{i+1} = g_i + P_i C_i$

$C_1 = g_0 + P_0 C_0 \quad \therefore C_2 = g_1 + P_1 C_1$ — 3

$= g_1 + P_1 (g_0 + P_0 C_0)$

$= g_1 + P_1 g_0 + P_1 P_0 C_0$

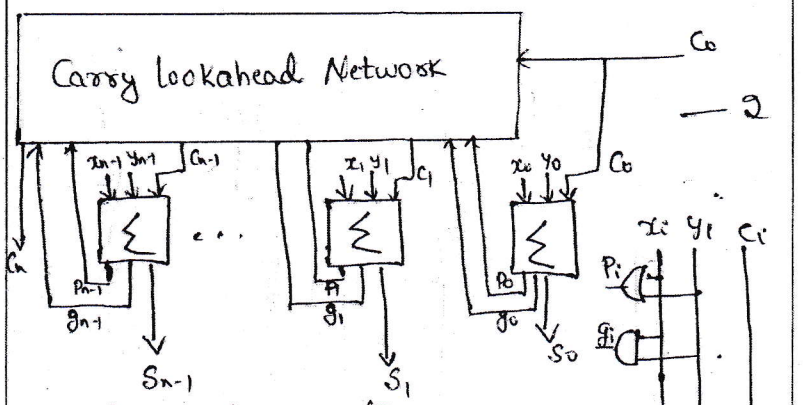
Similarly

$C_3 = g_2 + P_2 g_1 + P_2 P_1 g_0 + P_2 P_1 P_0 C_0$

$C_4 = g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0 + P_3 P_2 P_1 P_0 C_0$

$C_{i+1} = g_i + P_i g_{i-1} + P_i P_{i-1} g_{i-2} + \cdots + P_i P_{i-1} \cdots P_1 g_0 + P_i P_{i-1} \cdots P_0 C_0$

10



— 2

fig ④ General organization

fig ⑤ Sigma block

Explanation on Carry ripple Effect is eliminated — ④

Naveen Kumar S
Course in charge

Module Coordinator

HOD

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
SECOND INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET: A

USN | | | | | | | | | | |

Degree : B.E
Branch – Stream : ECE
Course Title : Digital System Design using Verilog
Duration : 1 Hr (60 minutes)

Semester : III
Course Type / Code : BEC302
Date : 09/2/2024
Max Marks : 25

Note: Answer **ONE full** question from each module

K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 3			
1(a)	Write the Truth Table of 3:8 line decoder using OR gates. **Develop** following Boolean expressions using $f_1 = \Sigma\, m(1,3,4)$ $f_2 = \Sigma\, m(0,2,6,7)$ (a) 3:8 decoder and OR gates (b) 3:8 line decoder and NOR gates	5	CO3	K3
(b)	Explain 4:1 Multiplexer with logic diagram, truth table and expressions.	5	CO3	K2
	OR			
2(a)	**Construct** $D = \{a,b,c,d\} = \Sigma\, m(0,1,5,6,7,9,12,15)$ using 8:1 Multiplexer	5	CO3	K3
(b)	Explain the notations of PLDs for (a) Unprogrammed OR gate (b) Unprogrammed AND gate (c) Programmed and gate realizing the term ac (d) Special notation for an AND gate having all its input fuses intact (e) OR gate with non fusible inputs	5	CO3	K2
	Module 4			
3(a)	Explain Master Slave SR Flip Flop with logic diagram	5	CO4	K2
(b)	**Make use of** the logic diagram of Master slave SR Flip Flop from (a) and draw the timing diagram, logic symbol and truth table for the same.	5	CO4	K3
(c)	**Construct** the logic diagram of a Serial In Parallel Out unidirectional shift register and explain the same.	5	CO4	K3
	OR			
4(a)	**Explain** Master Slave D flip flop and Master Slave T Flip flop.	5	CO4	K2
(b)	**Apply** the concepts of flip flops to Derive the characteristics equations for JK flip flop and T flip flop.	5	CO4	K3
(c)	**Construct** and explain a Universal bidirectional Shift register.	5	CO4	K3

Name & Signature of Course In charge

Name & Signature of Module Coordinator

HOD

Principal

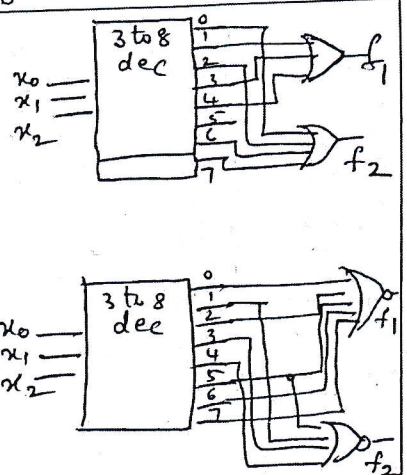
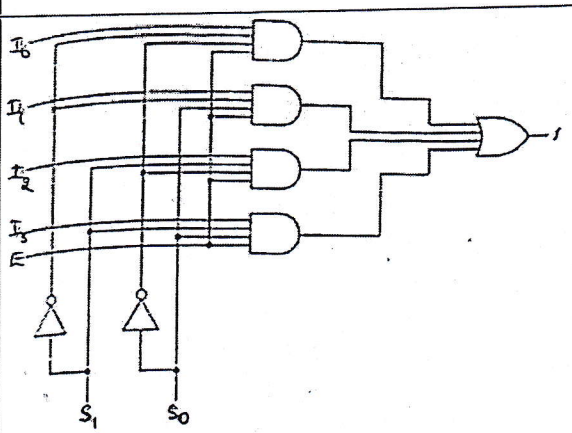
Selected

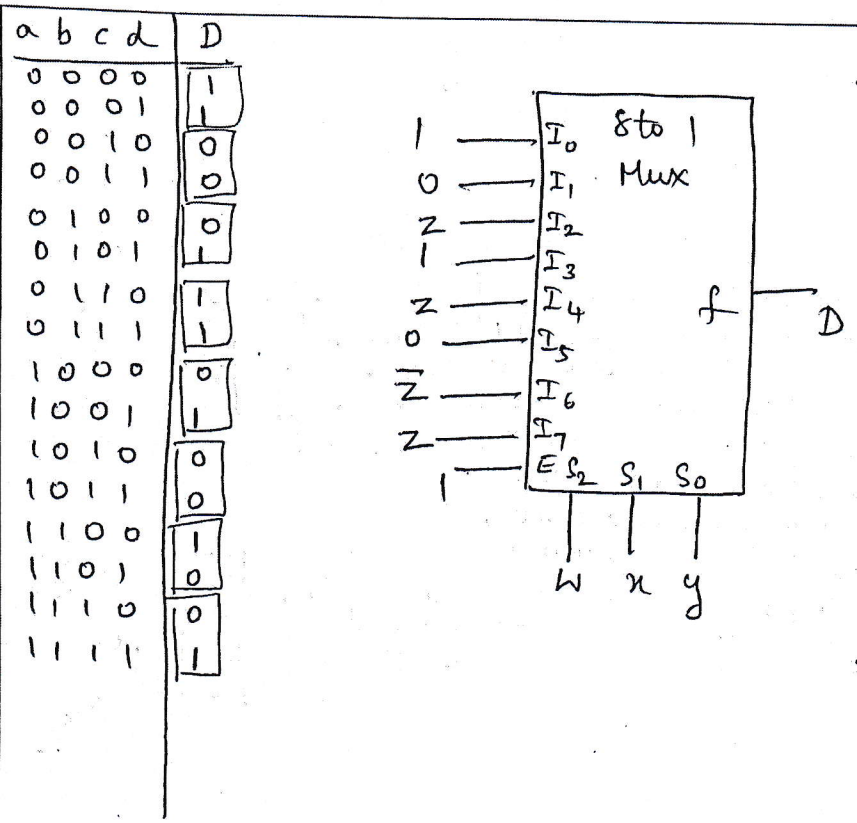
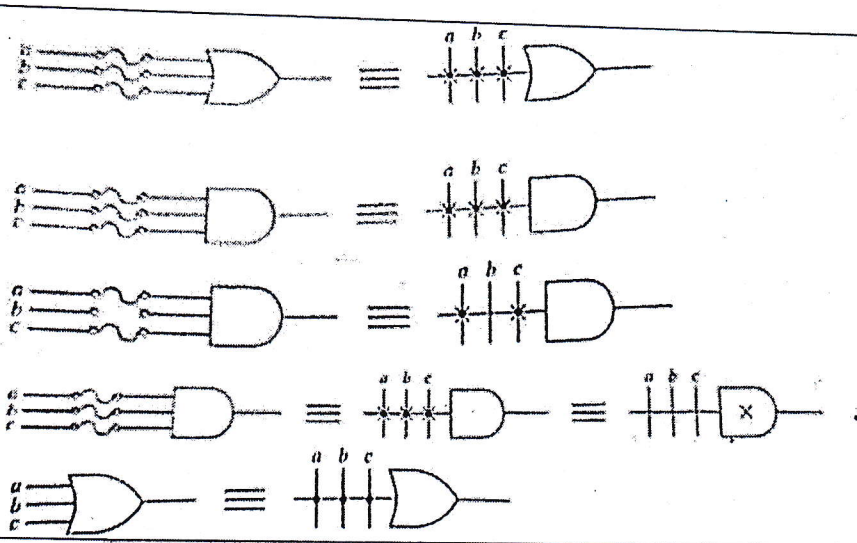
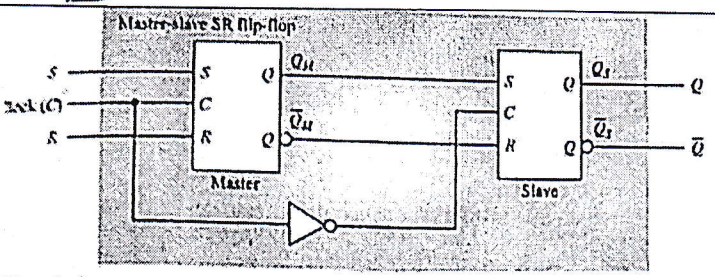
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
SECOND INTERNAL TEST QUESTION PAPER 2023 – 24 ODD SEMESTER

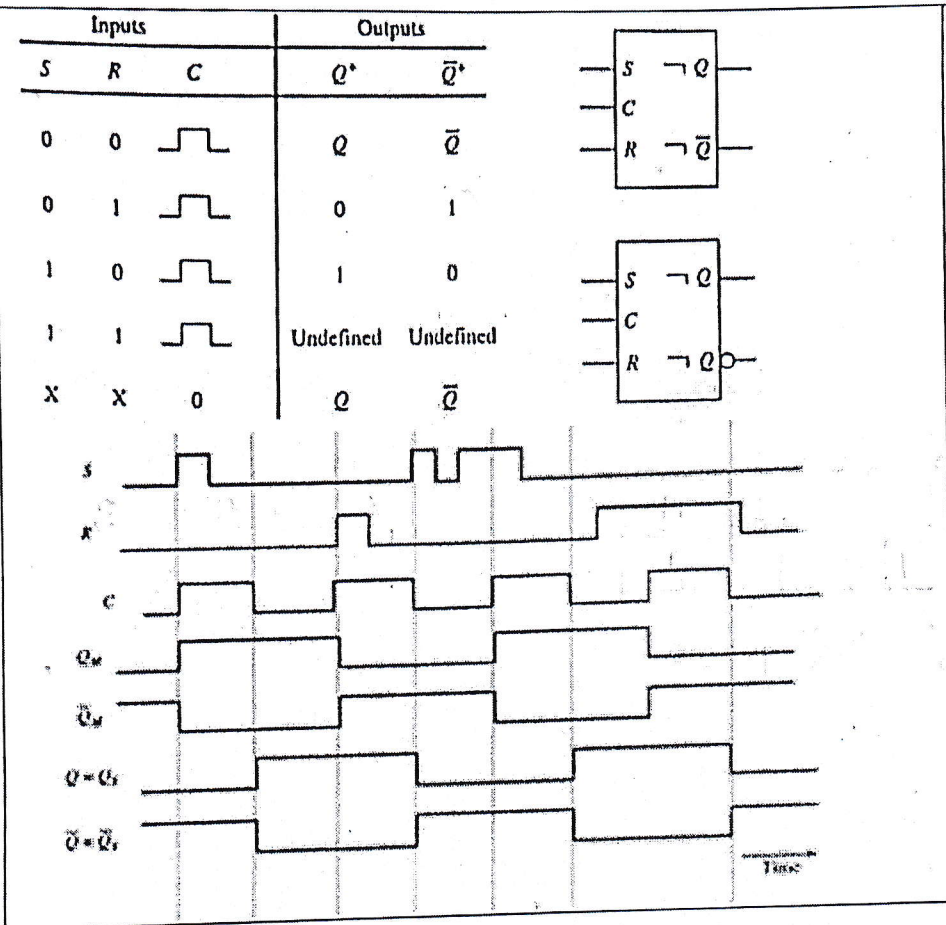
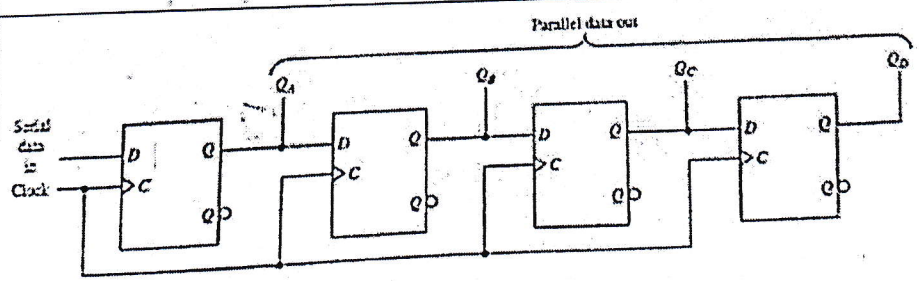
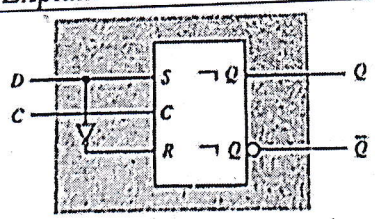
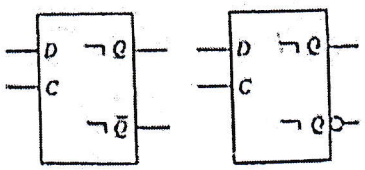
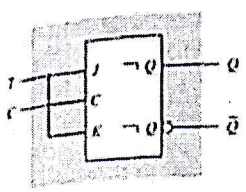
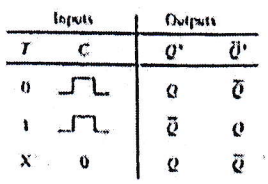
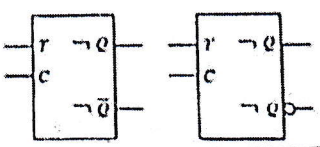
SCHEME AND SOLUTION (SET A)

Degree : B.E
Branch : ECE
Course Title : Digital System Design using Verilog

Semester : III A &B
Course Code : BEC302
Max Marks : 25

Q.NO.	POINTS	MARKS
1 (a)	$x_2\ x_1\ x_0$ | $z_7\ z_6\ z_5\ z_4\ z_3\ z_2\ z_1\ z_0$ 0 0 0 | 0 0 0 0 0 0 0 1 0 0 1 | 0 0 0 0 0 0 1 0 0 1 0 | 0 0 0 0 0 1 0 0 0 1 1 | 0 0 0 0 1 0 0 0 1 0 0 | 0 0 0 1 0 0 0 0 1 0 1 | 0 0 1 0 0 0 0 0 1 1 0 | 0 1 0 0 0 0 0 0 1 1 1 | 1 0 0 0 0 0 0 0  	5
1 (b)	 $E\ S_1\ S_0\ I_0\ I_1\ I_2\ I_3$ | f 0 × × × × × × | 0 1 0 0 0 × × × | 0 1 0 0 1 × × × | 1 1 0 1 × 0 × × | 0 1 0 1 × 1 × × | 1 1 1 0 × × 0 × | 0 1 1 0 × × 1 × | 1 1 1 1 × × × 0 | 0 1 1 1 × × × 1 | 1 Explain	5

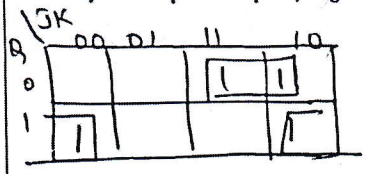
2(a)		5
2(b)		5
3 (a)	 Explain	5

3(b)		5
3(c)	 Explain	5
4(a)	  Explain   	5

4(b) — 5

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

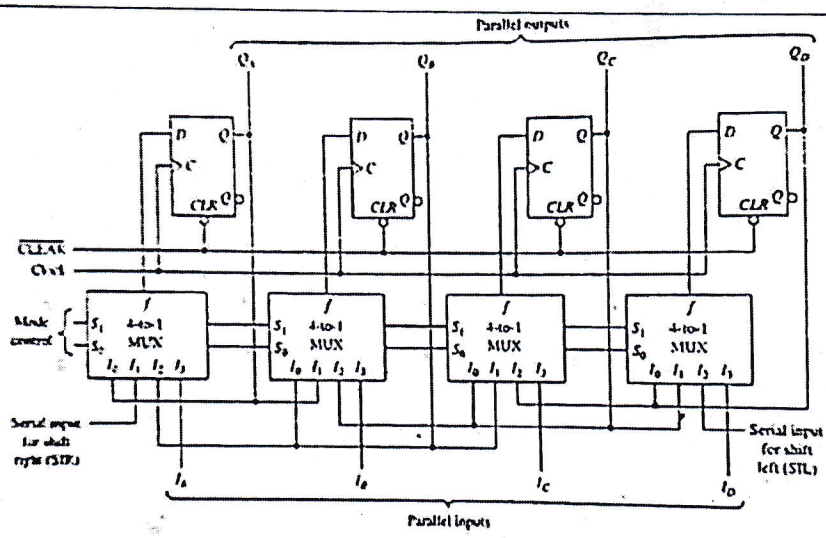


$Q^+ = J\bar{Q} + \bar{K}Q$

$Q^+ = T\bar{Q} + \bar{T}Q$

$= T \oplus Q$

4(c) — 5



Explain

Course in charge

Module Coordinator

HOD

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
SECOND INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET: B

USN | | | | | | | | | | |

Degree : B.E
Branch – Stream : ECE
Course Title : Digital System Design using Verilog
Duration : 1 Hr (60 minutes)

Semester : III
Course Type / Code : BEC302
Date : 05/02/2024
Max Marks : 25

Note: Answer **ONE full** question from each module

K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 3			
1(a)	**Make use of** Truth table of comparator to obtain the expression and logic diagram for $G_{i+1}, E_{i+1}, L_{i+1}$	5	CO3	K3
(b)	Write the Truth Table of 3:8-line decoder using NAND gates and **show** its Realization for the pair of maxterm canonical expressions $f_1 = \pi M(0,3,5)$ $f_2 = \pi M(2,3,4)$ using 3:8 decoder and two AND gates	5	CO3	K2
	OR			
2(a)	**Construct** $D = \{w, x, y, z\} = \Sigma m (0,1,2,4,5,7,8,9,12,13)$ using 8:1 Multiplexer	5	CO3	K3
(b)	**Make use of** Truth table of comparator and **explain** its function	5	CO3	K2
	Module 4			
3(a)	**Explain** Master Slave JK Flip Flop with logic diagram	5	CO4	K2
(b)	**Make use of** the logic diagram of Master slave JK Flip Flop and draw the timing diagram, logic symbol and truth table for the same	5	CO4	K3
(c)	**Explain** Parallel In unidirectional shift register and construct its logic diagram	5	CO4	K2
	OR			
4(a)	**Explain** Serial-in Serial-out Unidirectional shift register with block diagram	5	CO4	K2
(b)	**Apply** the concepts of flip flops to Derive the characteristics equations for SR flip flop and D flip flop.	5	CO4	K3
(c)	What are Registers. **Explain** any two classifications of registers	5	CO4	K2

Name & Signature of Course In charge

Name & Signature of Module Coordinator

HOD

Principal

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

II SESSIONAL TEST QUESTION PAPER 2023 – 24 ODD SEMESTER

SCHEME AND SOLUTION (SET B)

Degree	:	B.E	Semester	:	III
Branch	:	ECE	Course Code	:	BEC302
Course Title	:	DSDV	Max Marks	:	25

Q.NO.	POINTS	MARKS
1(a)	**Table 5.4** Truth table for a 1-bit comparator	5

A_i	B_i	G_i	E_i	L_i	G_{i+1}	E_{i+1}	L_{i+1}
0	0	0	0	0	–	–	–
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	✗	✗	✗
0	0	1	0	0	1	0	0
0	0	1	0	1	–	–	–
0	0	1	1	0	–	–	–
0	0	1	1	1	–	–	–
0	1	0	0	0	–	–	–
0	1	0	0	1	0	0	1
0	1	0	1	0	0	1	0
0	1	0	1	1	–	–	–
0	1	1	0	0	0	0	1
0	1	1	0	1	–	–	–
0	1	1	1	0	–	–	–
0	1	1	1	1	–	–	–
1	0	0	0	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	0	1	0	0
1	0	0	1	1	1	0	0
1	0	1	0	0	1	0	0
1	0	1	0	1	1	0	0
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	0	1	0
1	1	0	1	1	–	–	–
1	1	1	0	0	0	0	1
1	1	1	0	1	–	–	–
1	1	1	1	0	–	–	–
1	1	1	1	1	–	–	–

(2)

(2)

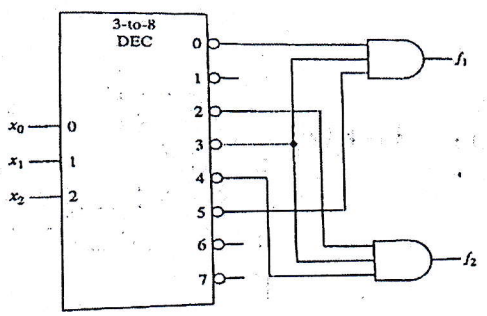
(1)

Logic diagram

Expression for $G_{i+1}, E_{i+1}, L_{i+1}$

1(b)

Inputs x_2	x_1	x_0	Outputs z_0	z_1	z_2	z_3	z_4	z_5	z_6	z_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

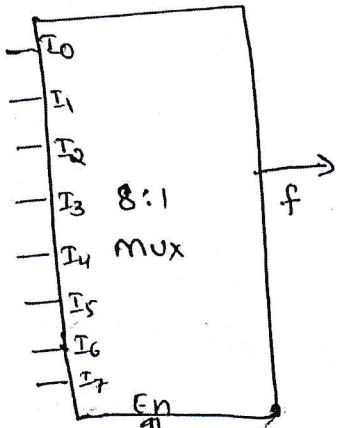


5

Truth table - 2

Realization - 3

2(a). Expressions
Finding input values – (3)



Realization using 8:1 mux – (2)

-5-

2(b)

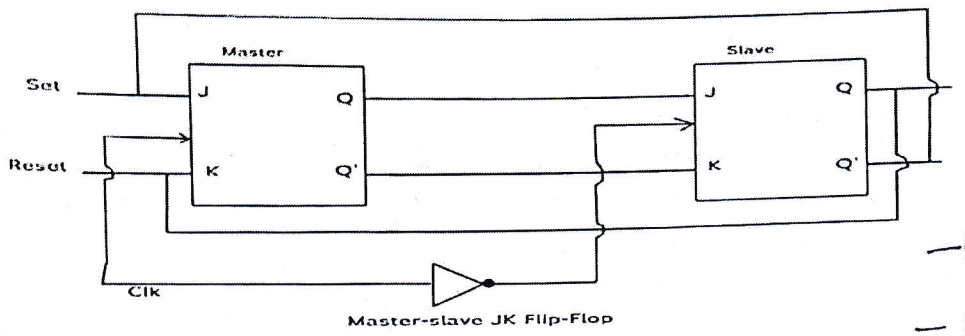
Table 5.4 Truth table for a 1-bit comparator

A_i	B_i	G_i	E_i	L_i	G_{i+1}	E_{i+1}	L_{i+1}	A_i	B_i	G_i	E_i	L_i	G_{i+1}	E_{i+1}	L_{i+1}
0	0	0	0	0	–	–	–	1	0	0	0	0	–	–	–
0	0	0	0	1	0	0	1	1	0	0	0	1	1	0	0
0	0	0	1	0	0	1	0	1	0	0	1	0	1	0	0
0	0	0	1	1	X	X	X	1	0	0	1	1	–	–	–
0	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0
0	0	1	0	1	–	–	–	1	0	1	0	1	–	–	–
0	0	1	1	0	–	–	–	1	0	1	1	0	–	–	–
0	0	1	1	1	–	–	–	1	0	1	1	1	–	–	–
0	1	0	0	0	–	–	–	1	1	0	0	0	–	–	–
0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
0	1	0	1	0	0	0	1	1	1	0	1	0	0	1	0
0	1	0	1	1	–	–	–	1	1	0	1	1	–	–	–
0	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0
0	1	1	0	1	–	–	–	1	1	1	0	1	–	–	–
0	1	1	1	0	–	–	–	1	1	1	1	0	–	–	–
0	1	1	1	1	–	–	–	1	1	1	1	1	–	–	–

-5-

Truth table – 3

Explanation – 2

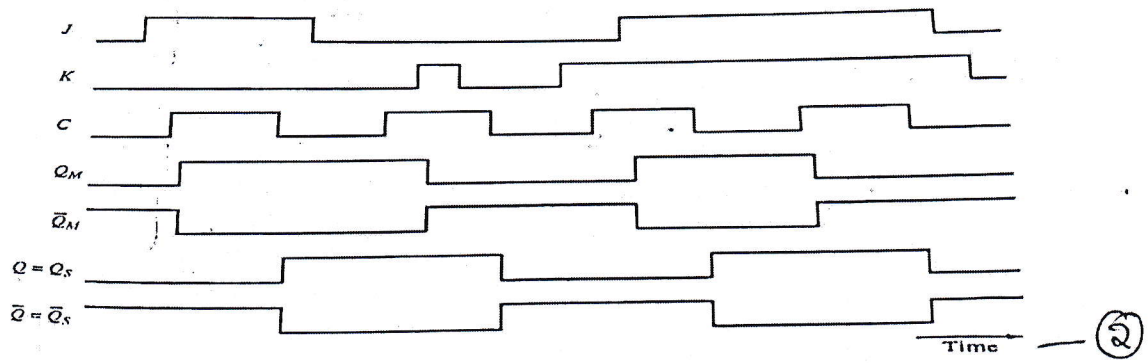


Master-slave JK Flip-Flop — (2)

— (3)

- 5 -

Explanation



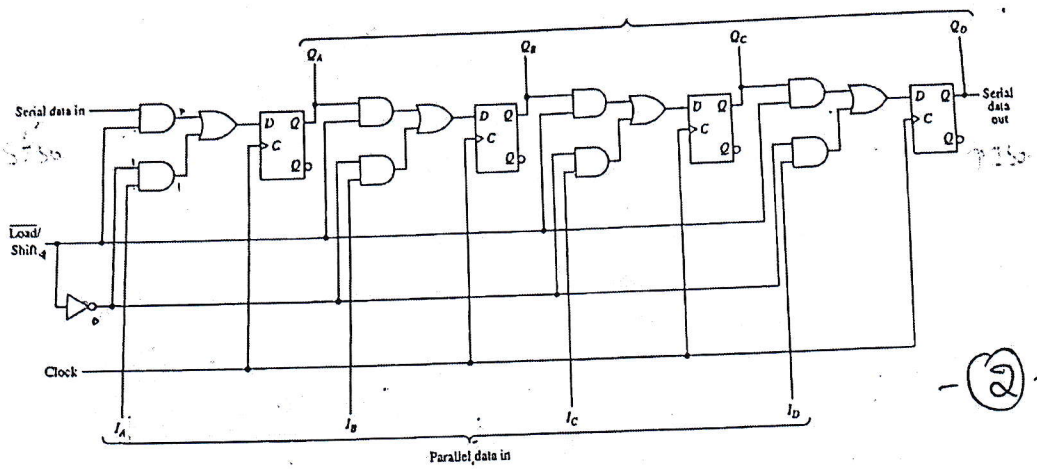
— (2)

- 5 -

Truth Table — (1)

Logic symbol + Explanation — (2)

3(c)



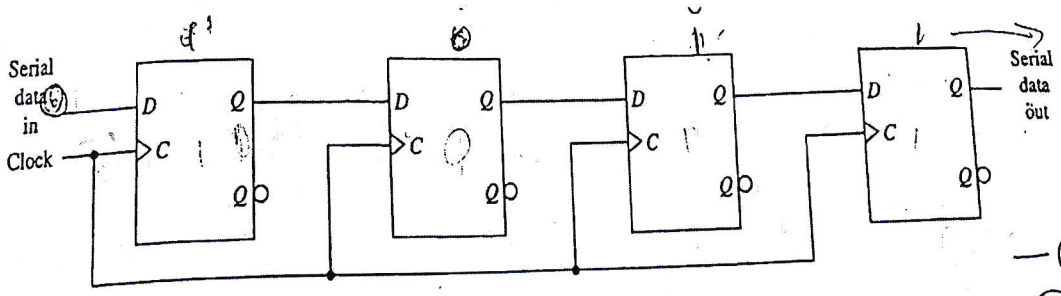
-(2)-

(5)

-(3)-

Explanation:

4(a)



-(2)- -5-

-(3)-

Explanation:

4(b)

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	—
1	1	1	—

} Inputs not allowed

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

-2-

-5-

-3-

Deriving Characteristic equation

(c)	Registers are the collection of flip-flops to store the binary values	– (1) –	– 5 –
	Explanation of any two shift registers SISO / Parallel-in shift Register / Universal Shift register	– (4)	

Naveen Kumar S
Signature of Course Incharge

Signature of Module Coordinator

Signature of HOD/ECE

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
THIRD INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET: A

USN | | | | | | | | | | |

Degree : B.E
Branch – Stream : ECE
Course Title : Digital System Design using Verilog
Duration : 1 Hr (60 minutes)

Semester : III
Course Type / Code : BEC302
Date : 04/03/2024
Max Marks : 25

Note: Answer **ONE full** question from each module

K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 4			
1	Develop a MOD 8 synchronous counter using clocked JK Flip Flops for sequence: 0-2-3-6-5-1	5	CO4	K3
	OR			
2	Develop and explain mod 8 twisted ring counter (Johnson counter) with the help of logic diagram and truth table.	5	CO4	K3
	Module 5			
3(a)	Explain the organization of behavioral description with an example	5	CO5	K2
(b)	Construct (Write) a Verilog code for 3 bit ripple carry adder using structural description.	5	CO5	K3
(c)	Construct (Write) a Verilog code for 4 bit counter with synchronous clear.	5	CO5	K3
(d)	Construct (Write) a Verilog code for 2:1 MUX using ELSE IF statement.	5	CO5	K3
	OR			
4(a)	Explain the following sequential statements in Verilog: if, for, repeat with examples	5	CO5	K2
(b)	Construct (Write) a Verilog code for 2:1 MUX using if-else statement.	5	CO5	K3
(c)	Construct / Write a Verilog code for priority encoder using casex.	5	CO5	K3
(d)	Construct (Write) a Verilog code for Half adder using structural description and explain the same.	5	CO5	K3

Name & Signature of Course In charge

Name & Signature of Module Coordinator

HOD

Principal

Selected

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
THIRD INTERNAL TEST QUESTION PAPER 2023 – 24 ODD SEMESTER

SCHEME AND SOLUTION (SET A)

Degree : B.E
Branch : ECE
Course Title : Digital System Design Using Verilog

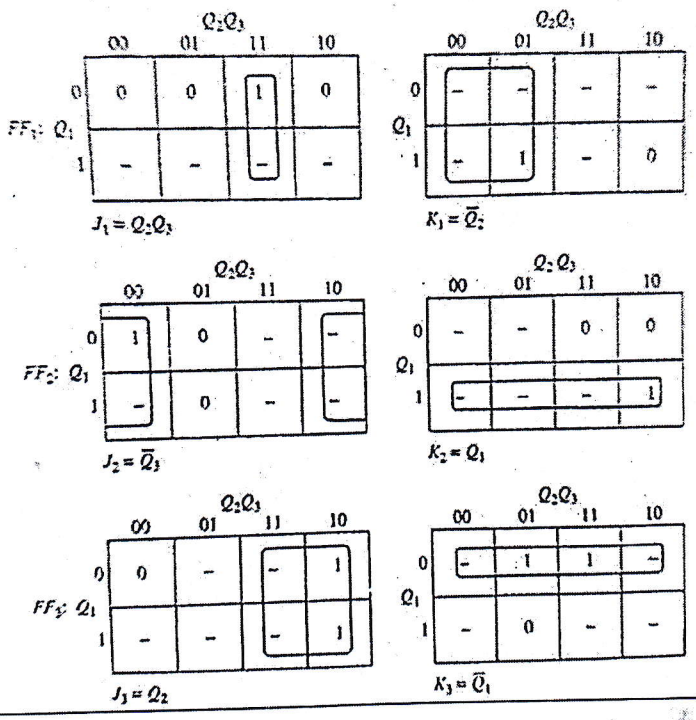
Semester : III A&B
Course Code : BEC302
Max Marks : 25

Q.NO.	POINTS	MARKS
1		5
2		5

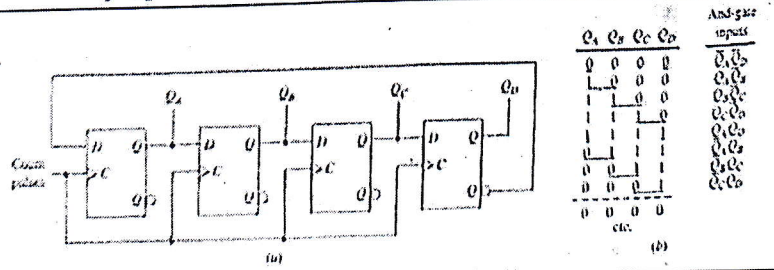
Q.1

Present state			Next state			Flip-flop inputs					
Q_1	Q_2	Q_3	Q_1^+	Q_2^+	Q_3^+	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	1	0	0	–	1	–	0	–
0	1	0	0	1	1	0	–	–	0	1	–
0	1	1	1	1	0	1	–	–	0	–	1
1	1	0	1	0	1	–	0	–	1	1	–
1	0	1	0	0	1	–	1	0	–	–	0
0	0	1	0	0	0	0	–	0	–	–	1

J K



Q.2



3(a)	Eg of half adder. Explanation on always statement, delays, execution	8
3(b)	module three_bit_adder (x, y, cin, sum, cout); input [2:0] x, y; input cin; output [2:0] sum; output cout; wire [1:0] carry; FULL_ADDER M0 (x[0], y[0], cin, sum[0], carry[0]); FULL_ADDER M1 (x[1], y[1], carry[0], sum[1], carry[1]); FULL_ADDER M2 (x[2], y[2], carry[1], sum[2], cout); /* It is assumed that the module FULL_ADDER (Listing 4.13) is attached by the simulator to the module three_bit_adder so, no need to rewrite the module FULL_ADDER.*/ endmodule	6

3(c)	module CNTR_LOP (clk, clr, q);
	input clk, clr;
	output [3:0] q;
	reg [3:0] q;
	integer i, j, result;
	initial
	begin
	q = 4'b0000; //initialize the count to 0
	end
	always @ (posedge clk)
	begin
	if (clr == 0)
	begin
	result = 0;
	//change binary to integer
	for (i = 0; i < 4; i = i + 1)
	begin
	if (q[i] == 1)
	result = result + 2**i;
	end
	result = result + 1;
	for (j = 0; j < 4; j = j + 1)
	begin
	if (result %2 == 1)
	q[j] = 1;
	else
	q[j] = 0;
	result = result/2;
	end
	end
	else q = 4'b0000;
	end
	endmodule
		6

3(d)	module MUXBH (A, B, SEL, Gbar, Y);
	input A, B, SEL, Gbar;
	output Y;
	reg Y; /* since Y is an output and appears inside always,
	Y has to be declared as reg (register) */
	
	always @ (SEL, A, B, Gbar)
	begin
	if (Gbar == 0 & SEL == 1)
	begin
	Y = B;
	end
	else if (Gbar == 0 & SEL == 0)
	Y = A;
	else
	Y = 1'bz; //Y is assigned to high impedance
	end
	
	endmodule	

4(a)	FOR statement syntax with example
	For (i=0; i<=5;i=i+1) begin
	Statements
	end
	IF statement syntax with example
	If (condition) begin
	Statements 1 end
	Else if (condition) begin
	Statements 2 end
	Else begin
	Statements 3 end
	REPEAT statement syntax
	Repeat (32)
	Begin
	#100 i=i+1;
	End
		8

4(b)	module mux2x1 (A, B, SEL, Gbar, Y);
	input A, B, SEL, Gbar;
	output Y;
	reg Y;
	always @ (SEL, A, B, Gbar)
	begin
	if (Gbar == 1)
	Y = 1'bz;
	else
	begin
	if (SEL)
	Y = B;
	else
	Y = A;
	end
	end
	
	endmodule
		6

4(c)

```
module Encoder_4 (Int_req, Rout_addrs);
input [3:0] Int_req;
output [3:0] Rout_addrs;
    reg [3:0] Rout_addrs;

always @ (Int_req)
            begin
                casex (Int_req)
                    4'bxxx1 : Rout_addrs=4'd1;
                    4'bxx10 : Rout_addrs=4'd2;
                    4'bx100 : Rout_addrs=4'd4;
                    4'b1000 : Rout_addrs= 4'd8;
                    default : Rout_addrs=4'd0;

                endcase
            end
endmodule
```

6

Figure 3.11 shows the simulation output of Listing 3.10.

Int_req	1111	1110	1000	0011	1100	0101	0000	0110
Rout_addrs	0001	0010	1000	0001	0100	0001	0000	0010

4(d)

Verilog Half Adder Description

```
module half_add (a, b, S, C);
input a, b;
output S, C;
xor (S, a, b);
and (C, a, b);
endmodule
```

Course in charge

Module Coordinator

HOD

K.S. INSTITUTE OF TECHNOLOGY, BENGALURU - 560109
THIRD INTERNAL TEST QUESTION PAPER 2023-24 ODD SEMESTER

SET: B

USN | | | | | | | | | | |

Degree : B.E
Branch – Stream : ECE
Course Title : Digital System Design using Verilog
Duration : 1 Hr (60 minutes)

Semester : III
Course Type / Code : BEC302
Date : 04/03/2024
Max Marks : 25

Note: Answer **ONE full** question from each module

K-Levels: K1-Remebering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Q No.	Questions	Marks	CO	K-Level
	Module 4			
1	**Develop** a MOD 6 synchronous counter using clocked T Flip Flops for sequence: 0-2-3-6-5-1	5	CO4	K3
	OR			
2	**Develop** and explain Binary ripple counter with the help of logic diagram	5	CO4	K3
	Module 5			
3(a)	**Explain** the following sequential statements in Verilog: case, while, forever with examples	5	CO5	K2
(b)	**Construct** (Write) a Verilog code for positive edge triggered JK flipflop using case statement	5	CO5	K3
(c)	**Construct** (Write) a Verilog code for 3-bit binary counter using case statement	5	CO5	K3
(d)	**Construct** (Write) a Verilog code for Antidiuretic hormone mechanism	5	CO5	K3
	OR			
4(a)	**Explain** the organization of Structural description with an example	5	CO5	K2
(b)	**Construct** (Write) a Verilog code for 4-bit counter with synchronous hold	5	CO5	K3
(c)	**Construct** (Write) a Verilog code to find Factorial of a number using while loop	5	CO5	K3
(d)	**Construct** (Write) a Verilog code for Booth Algorithm to find the multiplication of two signed numbers	5	CO5	K3

Name & Signature of Course In charge

Name & Signature of Module Coordinator

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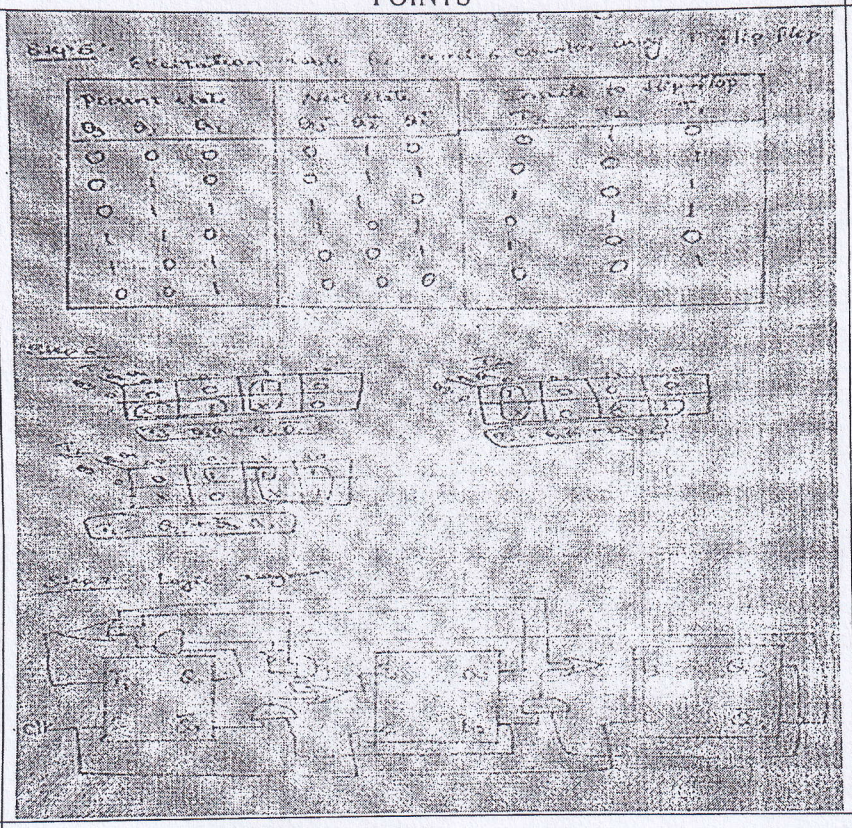
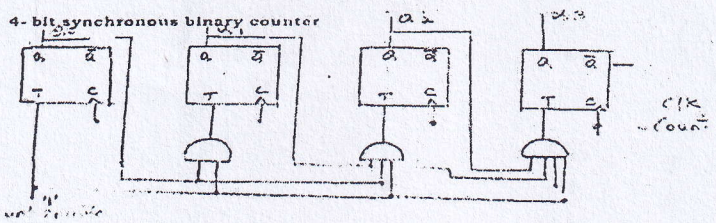
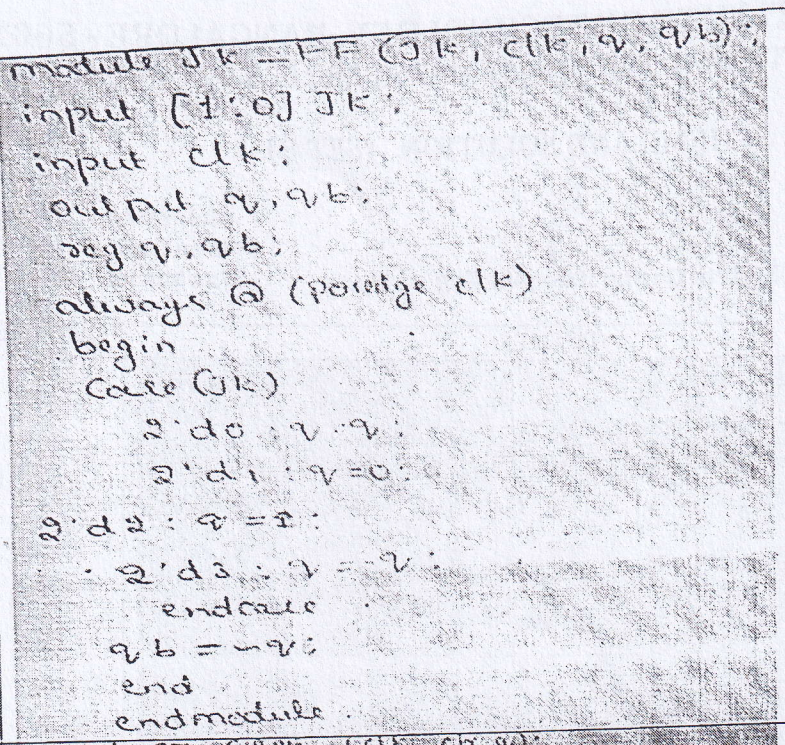
Principal

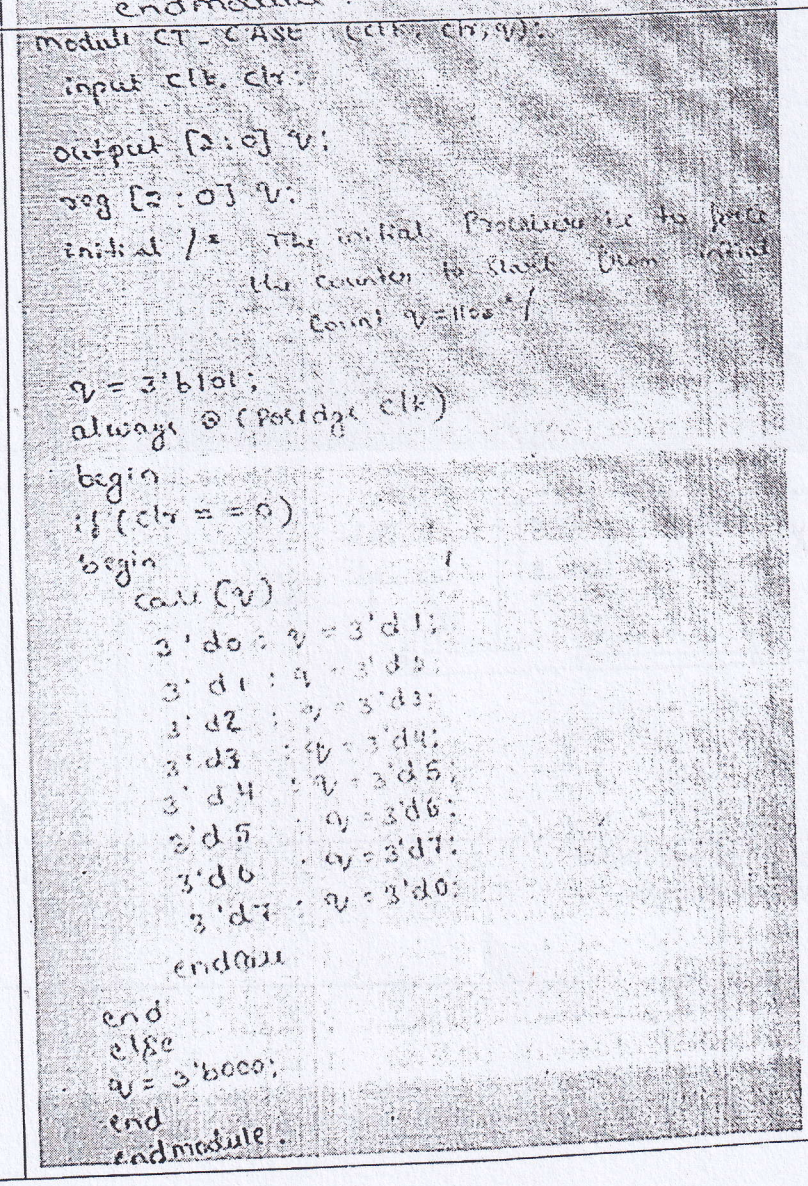
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
THIRD INTERNAL TEST QUESTION PAPER 2023 - 24 ODD SEMESTER

SCHEME AND SOLUTION (SET B)

Degree	:	B.E	Semester :	III A&B
Branch	:	ECE	Course Code :	BEC302
Course Title	:	Digital System Design Using Verilog	Max Marks :	25

Q.NO.	POINTS	MARKS
1		5
2	 Explanation	5
3(a)	Syntax for case, while and forever Explanation with an example	5

3(b)	 module JK_FF (JK, clk, q, qb);
	input [1:0] JK;
	input clk;
	output q, qb;
	reg q, qb;
	always @ (posedge clk)
	begin
	case (JK)
	2'd0 : q = q;
	2'd1 : q = 0;
	2'd2 : q = 1;
	2'd3 : q = ~q;
	endcase
	qb = ~q;
	end
	endmodule
		5

3(c)	 module CT_CASE (clk, clr, q);
	input clk, clr;
	output [2:0] q;
	reg [2:0] q;
	initial /* The initial Procedure is to force
	the counter to start from initial
	count q=1108 */
	q = 3'b101;
	always @ (posedge clk)
	begin
	if (clr == 0)
	begin
	case (q)
	3'd0 : q = 3'd1;
	3'd1 : q = 3'd2;
	3'd2 : q = 3'd3;
	3'd3 : q = 3'd4;
	3'd4 : q = 3'd5;
	3'd5 : q = 3'd6;
	3'd6 : q = 3'd7;
	3'd7 : q = 3'd0;
	endcase
	end
	else
	q = 3'b000;
	end
	endmodule
		5

4(b)

```
module CT_HOLD (CLK, hold, Q);
input clk, hold;
output [3:0] Q;
reg [3:0] Q;
integer i, result;
initial
begin
Q = 4'b0000; //initialize the count to 0
end
always @ (posedge CLK)
begin
result = 0;
// change binary to integer
for (i=0; i<=3; i=i+1)
begin
if (Q[i] == 1)
result = result + 8 * i;
end
result = result + 1;
for (i=0; i<=3; i=i+1)
begin
if (hold == 1)
i = 4; // to exit the loop
else
    begin
        if (result % 3 == 1)
        Q[i] = 1;
        else
        Q[i] = 0;
        result = result/3;
        end
end
end
endmodule
```

5

3(d)	module ADH (CIK, BP, ADH)
	input clk;
	input [8:0] BP;
	output reg [8:0] ADH;
	always @ (clk)
	begin
	if (clk == 1)
	begin
	if (BP <= 20) ADH = 100;
	else if (BP > 45.0) ADH = 0;
	else
	ADH = BP * (-4) + 180.0;
	end
	end
	endmodule
		5

4(a)	In the declaration part all the components used in the system description are declared. For example following description declares XOR gate component. **Component xor2** **port (i1, i2: in std_logic;o1:** **O1: out std_logic;** **end component;** The xor2 component has tow inputs "i1" and "i2", and one output "o1". Once the component is used we can use the same component one or more times in the system description. The instantiation part of the code maps the generic input/output to the actual input/output of the system. For example, the statement **X1: xor2 port map (A, B, sum) ;** Maps A to input I1 of xor2, input B to input i2 of xor2., and output sum to output o1 of xor2. This mapping means that the logic relationship between A,B and sum is same as between i1, i2 and o1. Verilog has a large number of built-in gates; for example the statement **Xor X1(sum, a , b);** Describes a two-input XOR gate, the inputs a and b, and the output is sum. X1 is an optional identifier for the gate; we can also write it as **Xor (sum, a ,b);** Verilog has a complete list of built-in primitive gates. The output of the gate sum has to be listed before the inputs a and b. Figure4.1 shows a list of gates and their code in Verilog **Program 4.1:HDL Structural Description—Verilog** **Verilog Structural Description** module system (a, b, sum, cout); input a, b; output sum, cout; xor X1 (sum, a, b); /* X1 is an optional identifier; it can be omitted.*/ and a1 (cout, a, b); /* a1 is optional identifier; it can be omitted.*/ endmodule	5

4(c)

```
module facm (N, Z);
input [5:0] N;
output [15:0] Z;
reg [15:0] Z;
integer i;
always @ (N)
begin
    Z = 1;
    i = 0;
    while (i < N)
      begin
        i = i + 1;
        Z = i * Z;
      end
end
endmodule
```

5

4(d)

```
module booth (
input signed [3:0] X, Y,
Output reg signed [7:0] Z,
reg [1:0] temp,
integer i;
reg E1
reg [3:0] Y1);
always @ (X, Y)
begin
Z = 8'd0;
E1 = 1'd0;
for (i=0; i<4; i=i+1)
begin
  temp = {X[i], E1};
          // The above statement is Concatenation.
  Y1 = -Y;
          // Y1 is 2's Complement of Y
Case (temp)
```

5

```
Case (temp)
8'd2 : z[7:4] = z[7:4] + Y1;
8'd1 : z[7:4] = z[7:4] + Y;
endcase
 z = z>>1;
      /* The above statement is a logical shift of one position to right */
 z[7] = z[6];
      /* The above two statements Perform arithmetic shift where the
         sign of the number is Preserved after the shift; */
 E1 = X[7];
 if (Y == 4'd8)

    begin
      z = -z;
    end
end
endmodule
```

Naveen Kumar S
Course in charge

Module Coordinator

HOD

DSDV IA Marks

OTAL IA MARKS = FINAL IA + ASSIGNMENT + DSDV LAB MARK

Sl. No	USN	Name of the Student	IA1 - 50	IA2 - 25	IA3 - 25	Avg IA - 15	Assignment (10)	IA + Assignment (25)	DSDV Lab (25)	Total IA (50)
1	1KS22EC071	NITHYASHREE V L	34	14	17	10	10	20	21	41
2	1KS22EC073	POOJA V	40	19	23	13	10	23	24	47
3	1KS22EC074	PRAJWAL P	45	18	16	12	10	22	25	47
4	1KS22EC075	PRANAV RAJATH	22	13	12	8	9	17	23	40
5	1KS22EC076	PREKSHITHA S	22	20	13	9	10	19	17	36
6	1KS22EC077	RACHANA JAGANNATH	30	19	12	10	10	20	22	42
7	1KS22EC078	RAGHU H M	29	23	22	12	10	22	25	47
8	1KS22EC079	RAKSHITA M B	10	17	10	6	10	16	22	38
9	1KS22EC080	RANJITH GOWDA K	19	17	13	8	10	18	21	39
10	1KS22EC081	ROHITH D YADAV	40	14	13	11	10	21	22	43
11	1KS22EC082	ROHITH M	40	20	19	12	10	22	24	46
12	1KS22EC083	SACHIN BASAPPA BABANNAVAR	33	19	14	10	10	20	22	42
13	1KS22EC084	SAHANA K R	26	16	15	9	10	19	21	40
14	1KS22EC085	SAHANA N R	29	9	11	8	10	18	22	40
15	1KS22EC086	SAHANA T BASANAGOUDRA	29	16	12	9	10	19	21	40
16	1KS22EC087	SARIKA S	19	8	12	6	10	16	21	37
17	1KS22EC088	SHALINI S	37	15	6	9	10	19	22	41

18	1KS22EC089	SHASHANK C	21	14	18	8	10	18	22	**40**
19	1KS22EC090	SHILPA T R	40	17	19	12	10	22	24	**46**
20	1KS22EC091	SHRAVANI G V	41	23	20	13	10	23	23	**46**
21	1KS22EC092	SHREE HARSHITHA S	35	9	15	9	10	19	21	**40**
22	1KS22EC093	SIDDHARTH SHARMA	30	19	24	11	10	21	23	**44**
23	1KS22EC094	SINCHANA S S	25	16	10	8	10	18	21	**39**
24	1KS22EC095	SNEHA	37	22	22	13	10	23	24	**47**
25	1KS22EC096	SOUMYASHREE F SARAF	14	11	9	6	10	16	21	**37**
26	1KS22EC097	SOWJANYA RAI	42	14	22	12	10	22	22	**44**
27	1KS22EC098	SPOORTHY B	36	22	16	12	10	22	22	**44**
28	1KS22EC099	SRUJAN H G	25	16	10	8	10	18	22	**40**
29	1KS22EC100	SRUJAN KARANTH N	36	20	19	12	10	22	24	**46**
30	1KS22EC101	SULAGNA MONDAL	44	20	21	13	10	23	24	**47**
31	1KS22EC102	SUMANJALI K	46	23	24	14	10	24	23	**47**
32	1KS22EC103	SUNITA SHIVASHANKAR SALOTAGI	34	15	12	10	10	20	22	**42**
33	1KS22EC104	SURYA R V	12	10	12	6	10	16	19	**35**
34	1KS22EC105	SWATHI S	20	10	4	6	7	13	17	**30**
35	1KS22EC106	TEJASWINI R	26	9	16	8	10	18	22	**40**
36	1KS22EC107	THANUSHREE M K	12	11	13	6	10	16	21	**37**
37	1KS22EC108	TIRUMALA GANESH BHARADWAJ SHARMA	22	10	2	6	10	16	22	**38**

38	1KS22EC109	UMME SARA	45	23	25	14	10	24	25	**49**
39	1KS22EC110	V LIKHITH	37	9	7	8	10	18	23	**41**
40	1KS22EC111	VARDHAN GOWDA K N	31	16	11	9	10	19	22	**41**
41	1KS22EC112	VARSHA B C	27	21	7	9	10	19	20	**39**
42	1KS22EC113	VARSHINI S	36	20	18	12	10	22	23	**45**
43	1KS22EC114	VARUN	23	17	18	9	10	19	25	**44**
44	1KS22EC115	VARUN RAYAPATI R	19	18	16	8	10	18	22	**40**
45	1KS22EC116	VEDASHREE M	39	17	23	12	10	22	25	**47**
46	1KS22EC117	VIDYASHREE H	24	19	15	9	10	19	21	**40**
47	1KS22EC118	VIJAYKUMAR SHANMUKHAYYA NAVALAGIMATH	11	14	12	6	10	16	18	**34**
48	1KS22EC119	VIKAS K S	35	21	24	12	10	22	25	**47**
49	1KS22EC120	VISHWANATH B S	30	18	13	10	9	19	18	**37**
50	1KS22EC121	VISHWANATH VEERAPUR	23	6	13	7	10	17	22	**39**
51	1KS22EC122	VISHWAS M K	37	11	13	10	10	20	22	**42**
52	1KS22EC123	VIVEK M S	27	7	17	8	10	18	22	**40**
53	1KS22EC124	VIVEK RAJ B	32	13	16	10	10	20	25	**45**
55	1KS22EC126	YASHWANTH P V	10	9	16	6	10	16	20	**36**
56		BHAVAN M	30	5	2	6	10	16	20	**36**
57		CHETHAN B L	23	8	7	6	10	16	20	**36**
58		CHINMAYI R	24	10	AB	6	10	16	22	**38**

60		HARISH N	23	8	7	6	10	16	19	**35**
61		HARSHITH M K	15	7	14	6	10	16	19	**35**
62		MANOJ R	28	8	1	6	10	16	21	**37**
64		NIKHIL M S	24	10	0	6	10	16	21	**37**
65		VIJAY D S	20	14	7	7	10	17	22	**39**
66		VIKAS GOWDA B S	21	10	5	6	10	16	19	**35**

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-5600109

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

2023-24 ODD SEMESTER

KSIT

List of students who are identified as slow learners and their marks in every internal

Subject and Subject Code: DIGITAL SYSTEM DESIGN USING VERILOG, BEC302

Semester and Section: III 'B'

Sl No.	USN	NAME	First Test Marks	Remedial Class Dates & Attendance		Improvement Test Marks	Second Test Marks	Remedial Class Dates & Attendance		Improvement Test Marks	Third Test Marks	Improvement Test Marks	FINAL
				9/1	16/1			10/2	16/2				
01	1KS22EC079	RAKSHITA M B	10	P	P		17	P	P		10	10	6
02	1KS22EC096	SOUMYASHREE F SARAF	14	P	P		11	P	P		4	9	6
03	1KS22EC104	SURYA R V	12	P	P		10	P	P		10	12	6
04	1KS22EC105	SWATHI S	8	P	P		10	P	P				
05	1KS22EC108	TIRUMALA GANESH BHARADWAJ SHARMA	Ab			22	10				2		6
06	1KS22EC118	VIJAYKUMAR SHANMUKHAYYA	11				7			14	12		6
07	1KS22EC126	YASHWANTH P V	Ab/10	P	P		9	P	P		16		6

Signature of the Faculty

Signature of the HOD

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

DEARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING AND LEARNING

PEDAGOGY REPORT

Academic Year	**2023-24 (ODD)**
Name of the Faculty	**Mrs. Bhargavi Ananth**
Course Name /Code	**Digital System Design Using Verilog (BEC302)**
Semester/Section	**III B**
Activity Name	**Code debugging**
Topic Covered	**Verilog dataflow, behavioral, structural description**
Date	**19/2/2024 to 24/2/2024**
No. of Participants	**66**
Objectives/Goals	• **To improve the debugging and analyzing skills in students** • **To improve the communication skills of students.**
ICT Used	**Xilinx**
Appropriate Method/Instructional materials/Exam Questions • **Initially delivered lecture on given topics.** • **Later students were given a set of 5 Verilog codes with errors. They had to run the code in Xilinx tool and correct the errors.**	
Relevant PO's	4,10
Significance of Results/Outcomes	• **Students put an effort to analyze the problems and solve them.**
Reflective Critique	• **Students improved their analyzing skills.** **Students improved their communication skills by making a report.**

Proofs (Photographs/Videos/Reports/Charts/Models)

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakpura main road, Bengalore - 560109

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
2022 -SCHEME

SUBJECT : DIGITAL SYSTEM AND DESIGN USING VERILOG [BEC302]

TOPIC : CODE DEBUGGING

NAME: UMME SARA

USN: 1KS22EC109

SEMESTER: 3rd

SECTION : B

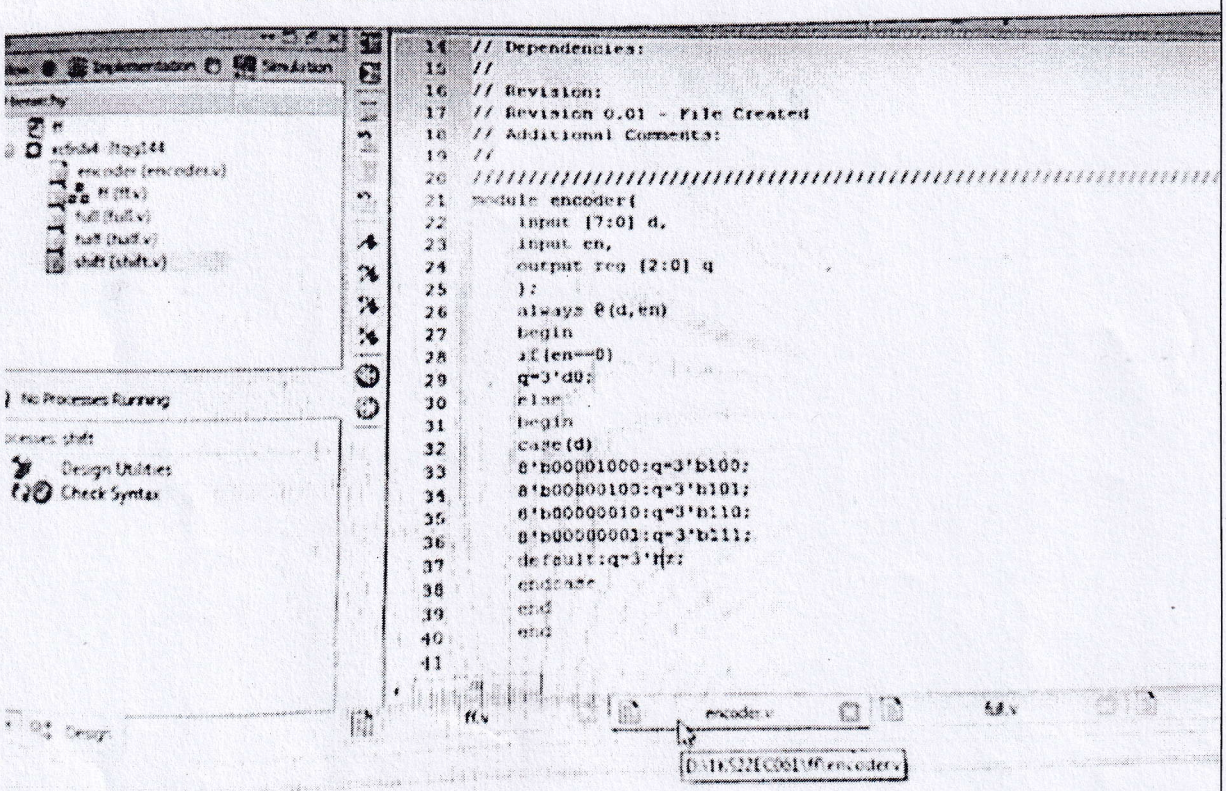
DATE : 24/02/2024

ERROR PROGRAM

4. 8:3 ENCODER

```
module Encoder(d0,d1,d2,d3,d4,d5,d6,d7,a,c);
input d0,d1,d2,d3,d4,d5,d6,d7;
output a,c;
or(a,d4,d5d6,d7);
or(b,d2,d3,d6,d7);
dor(c,d1,d3,d5,d7);
 endmodule;
```

SOLVED PROGRAM



Signature of Course In charge **Signature of HOD ECE**

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

DEARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING AND LEARNING

Content Beyond Syllabus

Academic Year	2023-24 (ODD)
Name of the Faculty	Mrs. Bhargavi Ananth
Course Name /Code	Digital System Design Using Verilog (BEC302)
Semester/Section	III B
Activity Name	Code debugging
Topic Covered	Verilog dataflow, behavioral, structural description
Date	19/2/2024 to 24/2/2024
No. of Participants	66
Objectives/Goals	• To improve the debugging and analyzing skills in students • To improve the communication skills of students.
ICT Used	Xilinx
Appropriate Method/Instructional materials/Exam Questions • Initially delivered lecture on given topics. • Later students were given a set of 5 Verilog codes with errors. They had to run the code in Xilinx tool and correct the errors.	
Relevant PO's	4,10
Significance of Results/Outcomes	• Students put an effort to analyze the problems and solve them.
Reflective Critique	• Students improved their analyzing skills. Students improved their communication skills by making a report.

Proofs (Photographs/Videos/Reports/Charts/Models)

K. S. INSTITUTE OF TECHNOLOGY

#14, Raghuvanahalli, Kanakpura main road, Bengalore - 560109

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
2022 -SCHEME

KSIT
K S INSTITUTE OF TECHNOLOGY

SUBJECT : DIGITAL SYSTEM AND DESIGN USING VERILOG [BEC302]

TOPIC : CODE DEBUGGING

NAME: UMME SARA

USN: 1KS22EC109

SEMESTER: 3rd

SECTION : B

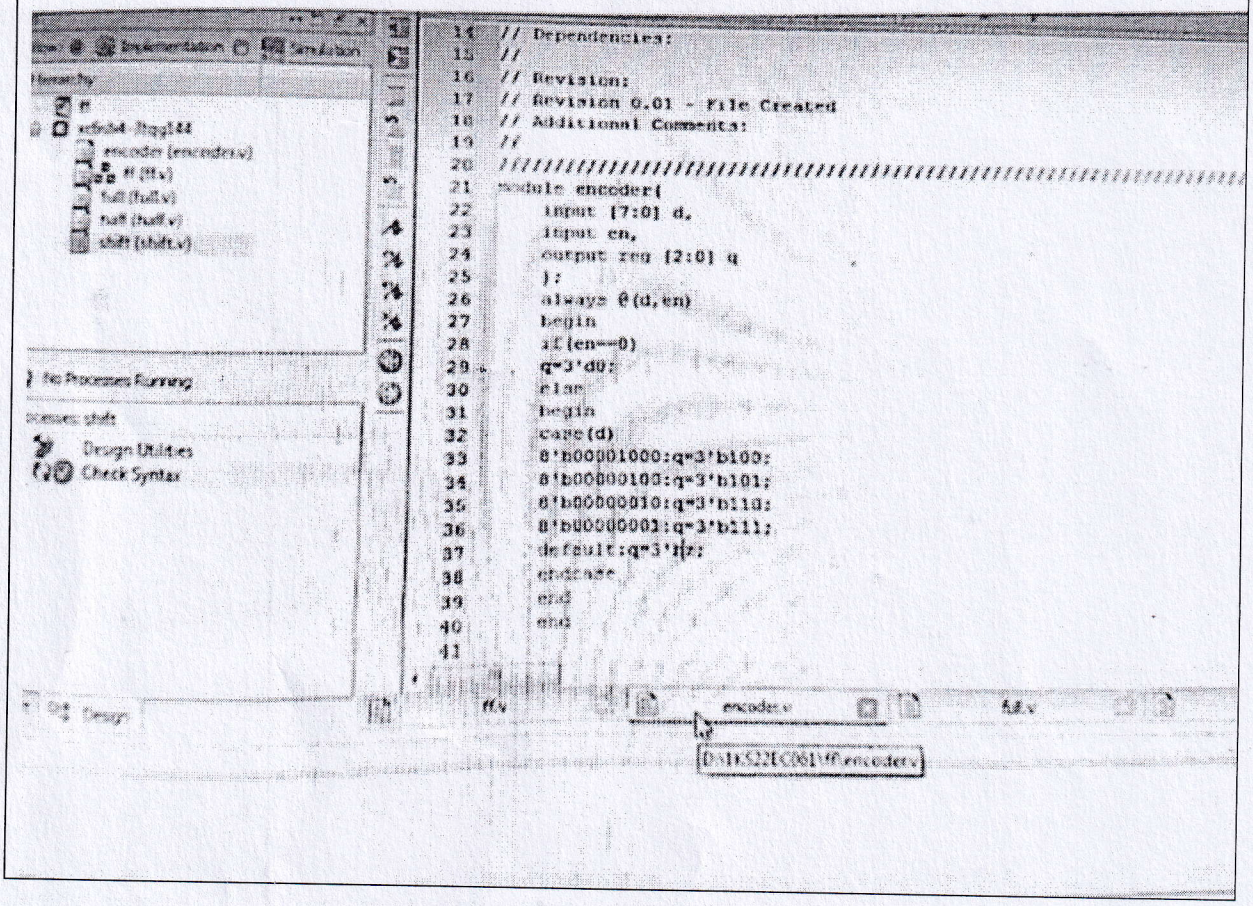
DATE : 24/02/2024

ERROR PROGRAM

4. 8:3 ENCODER

```
module Encoder(d0,d1,d2,d3,d4,d5,d6,d7,a,c);
input d0,d1,d2,d3,d4,d5,d6,d7;
output a,c;
or(a,d4,d5d6,d7);
or(b,d2,d3,d6,d7);
dor(c,d1,d3,d5,d7);
 endmodule;
```

SOLVED PROGRAM



Signature of Course In charge

Signature of HOD ECE

CBCS SCHEME

USN | | | | | | | | | | |

21EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What are combinational circuits? Give example. Explain combinational circuit with block diagram. (04 Marks)

b. Define canonical form representation and solve the following equation using canonical form:
i) P = f(a,b,c) = ab′ + ac′ + bc
ii) G = f(w,x,y,z) = w′x + yz′. (08 Marks)

c. Simplify the following Boolean function using K – Map
i) D = f(x, y, z) = Σm(0, 2, 4, 6)
ii) K = f(a, b, c) = Σm(1, 2, 3, 6, 7). (08 Marks)

OR

2 a. Define K-Map solve the following expression using K – Map.
i) K = f(w, x, y, z) = Σm(0, 1, 4, 5, 9, 11, 13, 15)
ii) D = f(a, b, c, d) = Σm(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14). (10 Marks)

b. Define Quine-McClusky method and solve the following Boolean expression using Quine-McClusky method.
i) D = f(a, b, c, d) = Σm(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)
ii) K = f(w, x, y, z) = Σm(1, 3, 13, 15) + Σd(8, 9, 10, 11). (10 Marks)

Module-2

3 a. Explain binary Adders with K–map and logical representation of equations for SUM and CARRY. (06 Marks)

b. Explain carry look ahead Adder with General and Sigma block. (06 Marks)

c. Explain working of decimal adder with neat block diagram (take example of BCD addition) (08 Marks)

OR

4 a. What are comparator circuits? Explain 2-bit magnitude comparators. (08 Marks)

b. Realize the Boolean expression using 3 : 8 decoder and two OR gates
i) $f_1(x_2, x_1, x_0) = \Sigma m(1, 2, 4, 5)$
ii) $f_2(x_2, x_1, x_0) = \Sigma m(1, 5, 7)$. (06 Marks)

c. Implement D = (w, x, y, z) = Σm(0, 1, 2, 4, 5, 7, 8, 9, 12, 13) using 8 : 1 MUX (06 Marks)

Module-3

5 a. Write a note on Master Slave JK Flip-Flops with function table and timing diagram. (08 Marks)

b. What are Edge Triggered Flip-Flops. Explain positive edge Triggered and negative edge Triggered Flip-Flops. (06 Marks)

c. Write characteristic equation for : i) JK Flip-Flop ii) SR Flip-Flop. (06 Marks)

OR

6 a. Define Counters. Explain Binary Ripple counter with neat diagram. (08 Marks)
b. What are Registers? Explain any two classification registers with neat block diagram. (06 Marks)
c. Design synchronous MOD-6 counter using clocked JK Flip-Flops for sequences : 0 – 2 – 3 – 6 – 5 – 1. (06 Marks)

Module-4

7 a. Define HDL and types of HDL. Give structure of verilog module with example. (06 Marks)
b. Explain verilog logical operators with example. (06 Marks)
c. i) Write a note on verilog Data type
ii) Write verilog code for 8 × 1 MUX. (08 Marks)

OR

8 a. Give classification of Styles(Types) of description with example. (08 Marks)
b. Write verilog code for Full Adder. (06 Marks)
c. Write a note on Arithmetic and shift, Rotate relational operators with example. (06 Marks)

Module-5

9 a. Write a note on structure of Behavioural Description with example. (08 Marks)
b. Write a note on Signal Assignment and Variable Assignment with example. (06 Marks)
c. Write a note on sequential statement with example. (06 Marks)

OR

10 a. Write a verilog code for 2 × 1 MUX using if ELSE STATEMENT. (06 Marks)
b. Explain structural description with example. (08 Marks)
c. Explain structural description of 3-bit Ripple Carry Adder. (06 Marks)

* * * * *

K. S. INSTITUTE OF TECHNOLOGY
#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-5600109
DEPARTMENT OF ELECTRONICS &COMMUNICATION ENGINEERING

QUESTION BANK

Module 3

1)With a neat diagram explain Binary ripple counters

2)Explain Ring and Jhonson counter

3)Design a synchronous Mod -6 counter for the given sequence (any sequence and using JK/D/T/SR can be asked)

Module 5

1)Explain the structure of Behavioral description with an example

2)write a Verilog code for 2:1 Mux using IF-ELSE // ELSE-IF

3)Write a note on sequential statements with an example of case, for, while, if-else, repeat, forever

4)Explain the Behavioral description of positive edge triggered JK flipflop using case statement with truth table and simulation waveform

5)Explain the Behavioral description of 4-bit binary counter with active high synchronous clear

6)Explain the structure of Structural description with an example

7)Structural description of 3 bit ripple Carry adder

8)write a Verilog code for

i)4 bit counter with synchronous clear

ii)4 bit counter with synchronous hold

iii)Priority encoder using caseX with truth table

iv)factorial of a number using while loop

v)Booth algorithm for multiplication of two signed numbers

vi)Genotypes and phenotypes using case

K.S.Institute of Technology,Bangalore -109

Department of Electronics and Communication Engg

3rd sem Course End Survey 2023-24

Course :Digital System Design using Verilog **Course Code : BEC302**

1.What is your understanding on Principles of Combinational Logic and Quine McCluskey Method
2.What is your level of understanding of PLDs and MSI Components
3.What is your ability to apply the knowledge of Flip Flops in design of counters
4.What is your ability to apply the basic knowledge of Verilog to write simple programs
5.What is your ability to apply the knowledge of verilog programming to write programs for Flip Flops and counters

Date	USN	Name of the	semand	Faculty Name	Q1	Q2	Q3	Q4
3-6-2024	1KS22EC106	Tejaswini R	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-7-2024	1KS22EC095	SNEHA	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-8-2024	1KS22EC096	SOUMYA	3rd sem-B	Mrs. Bhargavi Ananth	2	3	3	3
3-9-2024	1KS22EC119	Vikas k s	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-10-2024	1KS22EC083	SACHIN B	3rd sem-B	Mrs. Bhargavi Ananth	3	3	2	3
3-11-2024	1KS22EC111	Vardhan Gowda K N	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-12-2024	1KS22EC110	V LIKHITH	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-13-2024	1ks22ec118	Vijaykumar	3rd sem-B	Mrs. Bhargavi Ananth	2	2	2	2
3-14-2024	1KS22EC094	Sinchana S S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	2	3
3-15-2024	1ks22ec103	Sunita S S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-16-2024	1KS22EC113	Varshini S	3rd sem-B	Mrs. Bhargavi Ananth	3	2	3	2
3-17-2024	1KS22EC082	Rohith M	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-18-2024	1KS23EC402	Chinmayi R	3rd sem-B	Mrs. Bhargavi Ananth	1	1	1	2
3-19-2024	1KS22EC120	Vishwanath BS	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-20-2024	1KS22EC112	Varsha BC	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-21-2024	1KS22EC115	Varun Rayapati	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-22-2024	1KS22EC125	Yashavantha s	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-23-2024	1KS22EC117	Vidya shree.H	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
3-24-2024	1KS22EC063	Meghana S R	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-25-2024	1KS22EC025	Chethan AG	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-26-2024	1KS22EC058	Madhu Haromuchad	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-27-2024	1KS22EC028	D N Mithun	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-28-2024	1KS22EC036	Gayathri devi B	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-29-2024	1KS22EC030	Darshan Gowda MK	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
3-30-2024	1KS22EC066	Monika.HN	3rd sem-A	Mrs. Bhargavi Ananth	1	1	1	1
3-31-2024	1KS22EC037	GEHENA BS	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-1-2024	1 KS22EC062	MANOJ KUMAR N	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-2-2024	1KS22EC008	AMULYA.M.N	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-3-2024	1KS22EC067	Monisha B N	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-4-2024	1KS22EC026	Chidambar Prabhak	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-5-2024	1KS22EC019	Avinash	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-6-2024	1KS22EC007	Amrutha p	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-7-2024	1KS22EC003	Adith	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-8-2024	1KS22EC070	Nisarga.M	3rd sem-A	Mrs. Bhargavi Ananth	2	2	2	2
4-9-2024	1KS22EC124	Vivek raj b	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
4-10-2024	1KS22EC016	ARCHANA S K	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-11-2024	1KS22EC086	Sahana T Basanago	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
4-12-2024	1KS22EC087	Sarika. S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
4-13-2024	1KS22EC021	BHOOMIKA D	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3

4-14-2024	1KS22EC027	Chinmay sheelvant	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-15-2024	1KS22EC085	Sahana N R	3rd sem-B	Mrs. Bhargavi Ananth	2	2	2	2
4-16-2024	1KS22ECC107	Thanushree MK	3rd sem-B	Mrs. Bhargavi Ananth	2	2	3	3
4-17-2024	1KS22EC088	Shalini S	3rd sem-B	Mrs. Bhargavi Ananth	3	2	3	3
4-18-2024	1KS22EC004	Adithya. S	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-19-2024	1KS22ECO18	Ashwini P	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-20-2024	1KS22EC040	G Deekshitha	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-21-2024	1KS22EC065	Mohammed Taha	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-22-2024	1KS22EC011	Ankita P Budni	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-23-2024	1KS22EC121	VISHWANATH V	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
4-24-2024	1KS22EC089	Shashank. C	3rd sem-B	Mrs. Bhargavi Ananth	3	2	3	3
4-25-2024	1KS22EC075	PRANAV RAJATH	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
4-26-2024	1KS22EC081	Rohith D Yadav	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	2
4-27-2024	1KS23EC403	Deekshith	3rd sem-B	Mrs. Bhargavi Ananth	2	2	2	2
4-28-2024	1KS22EC031	Deeksha S Reddy	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-29-2024	1KS22EC035	Gagana S	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
4-30-2024	1KS22EC078	Raghu H M	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-1-2024	1KS22EC050	KIRAN.G	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-2-2024	1ks22ec061	Manasa Chowdary	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-3-2024	1KS22EC068	Nallani Hema	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-4-2024	1KS22EC007	AKASH S	3rd sem-A	Mrs. Bhargavi Ananth	1	1	2	2
5-5-2024	1KS22EC009	Anagha K S	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-6-2024	1ks22ec064	Megharaj	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-7-2024	1KS22EC069	Neha.M	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3
5-8-2024	1KS22EC100	Srujan Karanth N	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-9-2024	1KS22EC114	Varun	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-10-2024	1KS22EC074	Prajwal P	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-11-2024	1KS22EC052	LAKSHMI M	3rd sem-A	Naveen Kumar S	3	3	3	2
5-12-2024	1KS22EC044	Inchara C	3rd sem-A	Naveen Kumar S	3	3	3	3
5-13-2024	1KS22EC032	Deeksha T S	3rd sem-A	Naveen Kumar S	3	3	3	3
5-14-2024	1KS22EC042	Harshan M J	3rd sem-A	Naveen Kumar S	3	3	3	3
5-15-2024	1KS22EC039	Gowtham m	3rd sem-A	Naveen Kumar S	3	3	3	3
5-16-2024	1KS22EC098	SPOORTHY B	3rd sem-B	Mrs. Bhargavi Ananth	3	2	2	3
5-17-2024	1KS22EC054	Lekhana B H	3rd sem-A	Naveen Kumar S	3	3	3	3
5-18-2024	1KS22EC049	Keerthana K	3rd sem-A	Naveen Kumar S	3	2	3	2
5-19-2024	1KS22EC046	Amarendra	3rd sem-A	Naveen Kumar S	3	3	2	3
5-20-2024	1KS22EC071	Nithyashree.V.L	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	2
5-21-2024	1KS22EC123	Vivek MS	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-22-2024	1KS22EC073	Pooja V	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-23-2024	1KS22EC001	Abinay	3rd sem-A	Naveen Kumar S	3	3	3	3
5-24-2024	1KS22ECO23	C.Harika	3rd sem-A	Naveen Kumar S	3	3	3	3
5-25-2024	1KS22EC099	Srujan H G	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
5-26-2024	1KS22EC033	Dinesh.N	3rd sem-A	Naveen Kumar S	3	3	3	3
5-27-2024	1KS22EC034	GAGAN V S	3rd sem-A	Naveen Kumar S	3	3	3	3
5-28-2024	1KS22EC047	KARTHIK D	3rd sem-A	Naveen Kumar S	3	3	3	3
5-29-2024	1KS22EC102	Sumanjali.k	3rd sem-B	Mrs. Bhargavi Ananth	3	2	3	2
5-30-2024	1KS22EC097	Sowjanya Rai	3rd sem-B	Mrs. Bhargavi Ananth	2	3	3	3
5-31-2024	1KS22EC092	Shree harshitha S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-1-2024	1KS22ECO41	Harish M V	3rd sem-A	Naveen Kumar S	3	3	3	3
6-2-2024	1KS22EC091	Shravani g v	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-3-2024	1KS22EC012	Anupriya T	3rd sem-A	Naveen Kumar S	3	3	3	3
6-4-2024	1ks223ec038	Deepasree Chowdar	3rd sem-A	Mrs. Bhargavi Ananth	3	3	3	3

6-5-2024	1KS22EC101	Sulagna Mondal	3rd sem-B	Mrs. Bhargavi Ananth	3	2	3	3
6-6-2024	1KS22EC043	HITHA SM	3rd sem-A	Naveen Kumar S	2	2	3	2
6-7-2024	1KS22EC010	Ankit prakash	3rd sem-A	Naveen Kumar S	2	2	2	2
6-8-2024	1KS22EC002	Adeeba Ismath	3rd sem-A	Naveen Kumar S	3	3	3	3
6-9-2024	1KS22EC045	K VAMSHIKRISHNA	3rd sem-A	Naveen Kumar S	3	3	3	3
6-10-2024	1Ks22EC093	Siddharth sharma	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-11-2024	1KS22EC048	Kavya G	3rd sem-A	Naveen Kumar S	3	3	3	3
6-12-2024	1ks22ec080	Ranjith gowda k	3rd sem-B	Mrs. Bhargavi Ananth	2	3	3	2
6-13-2024	1KS22EC109	Umme sara	3rd sem-B	Mrs. Bhargavi Ananth	1	2	2	1
6-14-2024	1KS22EC126	YASHWANTH PV	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-15-2024	1KS22EC014	Archana M	3rd sem-A	Naveen Kumar S	3	3	3	3
6-16-2024	1KS22EC013	ANUSHA MALIPATI	3rd sem-A	Naveen Kumar S	2	2	2	2
6-17-2024	1kS22EC005	Ajith D	3rd sem-A	Naveen Kumar S	3	3	3	3
6-18-2024	11	CHETAN SP	3rd sem-A	Naveen Kumar S	3	3	3	3
6-19-2024	1ks22ec104	Surya RV	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-20-2024	1KS22EC079	Rakshita	3rd sem-B	Mrs. Bhargavi Ananth	2	3	3	2
6-21-2024	1KS22EC076	Prekshitha S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-22-2024	1ks22ec059	M.sushmitha	3rd sem-A	Naveen Kumar S	3	3	3	3
6-23-2024	1KS22EC057	Madham Purushotha	3rd sem-A	Naveen Kumar S	3	3	3	3
6-24-2024	1KS22EC108	TIRUMALA GANESI	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
6-25-2024	1KS22EC015	Archana N	3rd sem-A	Naveen Kumar S	3	3	3	3
6-26-2024	1KS22EC022	C Rahul	3rd sem-A	Naveen Kumar S	3	3	3	3
6-27-2024	IKS22EC055	LOHITH YAADAV R	3rd sem-A	Naveen Kumar S	3	3	3	3
6-28-2024	IKS22EC029	Arun Chowdary.D	3rd sem-A	Naveen Kumar S	3	3	3	3
6-29-2024	1KS22EC051	Kishan v	3rd sem-A	Naveen Kumar S	3	3	3	3
6-30-2024	1KS22EC020	Ayyaji madhava hn	3rd sem-A	Naveen Kumar S	3	3	3	3
7-1-2024	1KS22EC077	Rachana Jagannath	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-2-2024	1KS22EC090	Shilpa T R	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-3-2024	1KS22EC116	VEDASHREE M	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-4-2024	1ks22ec017	Ashok	3rd sem-A	Naveen Kumar S	2	3	3	3
7-5-2024	1ks22ec060	Mallikarjun	3rd sem-A	Naveen Kumar S	3	3	3	3
7-6-2024	1KS23EC410	Vikas Gowda BS	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-7-2024	1KS23EC409	Vijay D S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-8-2024	1KS22EC084	Sahana KR	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
-9-2024	1ks23ec400	BHAVAN M	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-10-2024	1KS22EC105	Swathi s	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-11-2024	1KS23EC408	Nikhil M S	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-12-2024	1KS23EC401	Chethan B L	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-13-2024	1KS23EC405	Harshith mk	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
7-14-2024	1KS23EC406	Manoj R	3rd sem-B	Mrs. Bhargavi Ananth	3	3	3	3
					4	**3**	**2**	**2**
				Total	**131**	**131**	**131**	**131**
				%age	**96.95**	**97.71**	**98.47**	**98.47**
				Average	**97.71**			

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

YEAR / SEMESTER/BRANCH	II/111/ECE
COURSE TITLE	Digital System Design using Verilog
COURSE CODE	BEC302
ACADEMIC YEAR	2023-24

ttainment Level	Significance
Level 3	Atleast 60% of the students should have scored >= 60% of Total marks
Level 2	Atleast 55% of the students should have scored >= 60% of Total marks
Level 1	Atleast 50% of the students should have scored >= 60% of Total marks

sl.no	USN	Name of the student	IA1				IA2			IA3			Assignment						Lab Internals (IPCC)					Obtained CO wise marks					CIE	SEE
			CO1	CO2	CO3	IA1	CO3	CO4	IA2	CO4	CO5	IA3	Avg	CO1	CO2	CO3	CO4	CO5	CO1	CO2	CO3	CO4	CO5	CO1	CO2	CO3	CO4	CO5		
	Max Marks		20	20	10	50	10	15	25	5	20	25	10	2	2	2	2	2	5	5	5	5	5	10.0	10.0	10.0	10.0	10.0	50.0	50
1	1KS22EC001	ABINAY	7	9	2	18	8	9	17	4	15	19	10	2	2	2	2	2	4.1	4.2	4.5	4.6	4.1	7.2	7.6	8.0	8.6	9.0	41.0	23
2	1KS22EC002	ADEEBA ISMATH	14	15	10	39	10	14	24	5	20	25	10	2	2	2	2	2	4.8	5	5	4.9	5	8.9	10.0	10.0	9.8	10.0	49.0	41
3	1KS22EC003	ADITH PINNEPALLI	2	13	2	17	6	12	18	5	8	13	9	2	2	1	2	2	3.2	3.4	3.4	3.4	3.1	5.5	8.0	5.6	8.0	6.3	34.0	18
4	1KS22EC004	ADITHYA S	15	17	6	38	5	10	15	4	20	24	10	2	2	2	2	2	4.8	4.8	5	4.9	5	9.1	9.4	8.7	9.0	10.0	47.0	30
5	1KS22EC005	AJITH D	6	12	9	27	2	14	16	4	8	12	10	2	2	2	2	2	4	3.9	4	3.8	4.2	6.9	7.7	7.7	8.5	7.4	39.0	18
6	1KS22EC006	AKASH S	2	19	8	29	2	0	2	3	10	13	9	2	1	2	2	2	3	3	3.1	3	3.1	5.3	6.9	6.6	5.5	6.6	31.0	18
7	1KS22EC007	AMRUTHA P	7	12	7	26	8	10	18	5	11	16	10	2	2	2	2	2	3.8	3.8	3.7	3.6	3.9	6.9	7.6	8.0	7.9	8.0	39.0	37
8	1KS22EC008	AMULYA M N	13	16	5	34	10	14	24	5	18	23	10	2	2	2	2	2	4.8	4.8	4.8	4.8	4.9	8.8	9.2	9.1	9.7	9.6	47.0	42
9	1KS22EC009	ANAGHA K S	11	18	10	39	5	13	18	5	14	19	10	2	2	2	2	2	4.4	4.4	4.6	4.6	4.6	8.1	9.1	8.9	10.0	8.7	45.0	32
10	1KS22EC010	ANKIT PRAKASH	10	10	7	27	7	10	17	3	15	18	10	2	2	2	2	2	5	5	4.9	4.7	5	8.5	8.5	9.0	8.7	10.0	45.0	38
11	1KS22EC011	ANKITA BUDNI	11	18	8	37	5	12	17	3	18	21	9	2	1	2	2	2	4.8	4.8	4.6	4.7	4.8	9.0	8.5	8.6	9.0	9.5	45.0	25
12	1KS22EC012	ANUPRIYA T	19	13	8	40	9	15	24	5	20	25	10	2	2	2	2	2	4.5	4.5	4.5	4.3	4.5	9.4	8.5	9.1	9.3	9.5	46.0	31
13	1KS22EC013	ANUSHA MALIPATIL	7	12	2	21	5	13	18	5	14	19	10	2	2	2	2	2	3.8	3.7	3.9	3.7	3.4	6.9	7.5	7.0	8.4	7.5	38.0	28
14	1KS22EC014	ARCHANA M	14	13	7	34	7	14	21	5	20	25	10	2	2	2	2	2	4.8	4.8	4.8	4.7	4.7	8.9	8.8	8.9	9.6	9.7	46.0	32
15	1KS22EC015	ARCHANA N	12	17	8	37	10	13	23	5	20	25	10	2	2	2	2	2	4.9	4.8	5	5	5	8.7	9.4	9.7	9.7	10.0	48.0	35
16	1KS22EC016	ARCHANA S K	19	18	8	45	10	14	24	3	20	23	10	2	2	2	2	2	5	4.9	4.8	4.8	5	9.9	9.6	9.5	9.4	10.0	49.0	32
17	1KS22EC017	ASHOK	8	8	6	22	8	7	15	3	15	18	9	2	1	2	2	2	4.8	4.8	4.7	4.6	4.3	8.0	7.0	8.8	8.1	8.6	41.0	27
18	1KS22EC018	ASHWINI P	17	19	9	45	10	13	23	5	20	25	9	1	2	2	2	2	4.6	4.6	4.7	4.6	4.8	8.2	9.5	9.6	9.3	9.0	46.0	29
19	1KS22EC019	AVINASH	12	18	8	38	9	15	24	5	20	25	10	2	2	2	2	2	4.6	4.6	4.7	4.6	4.7	8.4	9.3	9.3	9.6	9.7	47.0	24
20	1KS22EC020	AYYAJI MADHAVA H N	15	10	6	31	10	12	22	5	17	22	10	2	2	2	2	2	4.6	4.5	4.8	4.5	4.5	8.9	8.0	9.2	9.1	9.1	45.0	28
21	1KS22EC021	BHOOMIKA D	8	5	8	21	8	14	22	4	10	14	10	2	2	2	2	2	4.4	4.4	4.5	4.6	4.8	7.6	7.2	8.9	9.3	8.3	42.0	32
22	1KS22EC022	C RAHUL	12	11	0	23	7	12	19	3	4	7	10	2	2	2	2	2	4.2	4.3	4.1	4	4.1	8.0	8.0	7.2	8.3	6.7	39.0	28
23	1KS22EC023	CHERUKURU HARIKA	11	9	7	27	8	14	22	3	18	21	10	2	2	2	2	2	4.5	4.5	4.5	4.6	4.8	8.2	7.9	8.8	9.2	9.5	44.0	37
24	1KS22EC024	CHETAN S P	11	9	6	26	0	8	8	3	17	20	9	1	2	2	2	2	4.6	4.6	4.3	4.4	4.8	7.3	8.0	7.2	9.0	9.4	41.0	30
25	1KS22EC025	CHETHAN A G	19	17	9	45	10	14	24	2	14	16	10	2	2	2	2	2	4.8	4.7	4.8	4.8	4.4	9.7	9.3	9.7	9.2	8.5	47.0	39
26	1KS22EC026	CHIDAMBAR PRABHAKAR	9	10	4	23	10	13	23	5	20	25	9	2	1	2	2	2	4.4	4.4	4.3	4.2	4.6	7.8	6.9	8.4	8.9	9.6	42.0	32
27	1KS22EC027	CHINMAY SHEELWANTH	5	5	8	18	10	11	21	5	11	16	10	2	2	2	2	2	4.4	4.6	4.4	4.4	3.8	7.2	7.4	10.0	8.8	7.5	41.0	28
28	1KS22EC028	D N MITHUN	13	14	6	33	6	9	15	3	20	23	10	2	2	2	2	2	4.4	4.4	4.4	4.4	4.5	8.4	8.5	8.2	8.2	9.5	43.0	25
29	1KS22EC029	DARAPANENI ARUN CHOWDARY	7	15	0	22	2	14	16	3	6	9	10	2	2	2	2	2	3.4	3.6	3.4	3.8	3	6.5	7.9	5.7	8.4	5.9	35.0	23
30	1KS22EC030	DARSHAN GOWDA M K	15	11	8	34	9	12	21	5	18	23	10	2	2	2	2	2	4.6	4.6	4.6	4.6	4.8	8.9	8.3	9.2	9.2	9.5	45.0	18
31	1KS22EC031	DEEKSHA S REDDY	9	7	2	18	10	8	18	5	14	19	10	2	2	2	2	2	4.5	4.3	4.5	4.5	4.6	7.9	7.4	9.0	8.5	8.7	42.0	19
32	1KS22EC032	DEEKSHA T S	10	10	8	28	6	8	14	3	15	18	10	2	2	2	2	2	4.2	4.4	4.3	4.4	4.6	7.7	7.9	8.4	8.1	8.9	41.0	36
33	1KS22EC033	DINESH N	3	17	0	20	3	6	9	5	14	19	9	2	2	2	1	2	3.6	3.7	3.8	3.7	3.8	6.1	8.3	7.0	6.4	7.9	36.0	22
34	1KS22EC034	GAGAN V S	16	9	2	27	5	14	19	5	9	14	9	2	2	2	2	1	4.2	4.1	4.4	4	4.4	8.6	7.5	7.5	8.9	6.0	39.0	28
35	1KS22EC035	GAGANA S	18	16	4	38	9	6	15	5	19	24	10	2	2	2	2	2	4.4	4.4	4.4	4.4	4.5	9.1	8.8	8.4	8.1	9.4	44.0	25
36	1KS22EC036	GAYATHRI DEVI B	10	13	3	26	5	10	15	4	14	18	10	2	2	2	2	2	4.5	4.4	4.6	4.5	4.6	8.0	8.4	7.8	8.6	8.7	42.0	22
37	1KS22EC037	GEHENA B S	10	16	8	34	10	13	23	3	19	22	10	2	2	2	2	2	4.6	4.5	4.6	4.4	4.7	8.1	8.9	9.3	8.8	9.6	45.0	30
38	1KS22EC038	GONUGUNTLA DEEPA SREE	6	13	0	19	7	13	20	4	10	14	10	2	2	2	2	2	4	4	4	4	4.2	6.9	8.0	7.1	8.6	7.0	38.0	29

39	1KS22EC039	GOWTHAM M	7	5	8	20	10	14	24	5	17	22	10	2	2	2	2	2	4	3.9	4.2	4.2	4.6	7.1	6.7	8.9	9.1	9.2	41.0	32
40	1KS22EC040	GUNTURU DEEKSHITHA	13	15	3	31	10	13	23	5	16	21	10	2	2	2	2	2	4.2	4.4	4.3	4.3	4.6	8.2	8.7	8.3	9.0	9.0	44.0	27
41	1KS22EC041	HARISH M V	13	13	6	32	8	6	14	5	13	18	9	1	2	2	2	2	4	4.7	4.6	4.7	4.8	7.7	8.7	8.7	8.4	8.8	43.0	22
42	1KS22EC042	HARSHAN M J	18	15	9	42	10	14	24	5	18	23	10	2	2	2	2	2	4.8	4.9	4.8	4.9	5	9.5	9.2	9.7	9.8	9.7	48.0	29
43	1KS22EC043	HITHA S M	13	19	9	41	8	15	23	5	20	25	10	2	2	2	2	2	4.8	4.7	4.8	4.7	4.8	8.8	9.6	9.4	9.7	9.8	48.0	30
44	1KS22EC044	INCHARA C	12	14	8	34	7	15	22	4	18	22	10	2	2	2	2	2	4.7	4.8	4.6	4.8	4.8	8.5	8.9	8.9	9.7	9.5	46.0	29
45	1KS22EC045	K VAMSHIKRISHNA	14	10	5	29	7	10	17	5	9	14	10	2	2	2	2	2	4.3	4.5	4.6	4.6	4.7	8.4	8.0	8.4	8.9	8.1	42.0	34
46	1KS22EC046	KANDRA AMARENDRA	14	13	3	30	2	9	11	5	6	11	10	2	2	2	2	2	3.9	3.8	3.8	3.8	3	8.0	7.0	6.6	7.9	5.9	36.0	18
47	1KS22EC047	KARTHIK D	6	6	6	18	7	10	17	5	13	18	10	2	2	2	2	2	4.6	4.4	4.6	4.5	4.5	7.5	7.3	8.6	8.8	8.5	41.0	28
48	1KS22EC048	KAVYA G	17	16	8	41	8	14	22	4	15	19	10	2	2	2	2	2	4.8	4.6	4.6	4.8	4.7	10.0	9.0	9.0	9.5	9.0	47.0	30
49	1KS22EC049	KEERTHANA K	17	19	8	44	10	15	25	5	20	25	10	2	2	2	2	2	5	5	5	4.8	5	10.0	9.9	9.7	9.8	10.0	50.0	22
50	1KS22EC050	KIRAN G	19	15	8	42	10	15	25	5	15	20	10	2	2	2	2	2	4.7	4.7	4.7	4.8	4.6	9.6	9.0	10.0	9.8	8.9	48.0	32
51	1KS22EC051	KISHAN V	11	10	8	29	6	13	19	5	13	18	10	2	2	2	2	2	4.5	4.5	4.6	4.6	4.6	8.2	8.0	8.7	10.0	8.6	44.0	37
52	1KS22EC052	LAKSHMI M	15	17	7	39	10	9	19	5	16	21	10	2	2	2	2	2	4.4	4.4	4.6	4.4	4.5	8.7	9.0	9.2	8.5	8.9	45.0	36
53	1KS22EC054	LEKHANA B H	15	3	0	18	6	12	18	2	15	17	9	1	2	2	2	2	4.2	4.2	4.3	4.4	4.2	7.5	6.7	7.2	8.5	8.5	39.0	27
54	1KS22EC055	LOHITH YAADAV R	12	15	5	32	8	15	23	5	14	19	10	2	2	2	2	2	4.6	4.4	4.7	4.6	4.6	9.0	8.7	8.7	9.6	8.7	45.0	31
55	1KS22EC057	MADHAM PURUSHOTHAM	4	11	4	19	4	9	13	5	12	17	10	2	2	2	2	2	3.7	3.8	3.8	3.7	3.8	6.3	7.5	7.0	7.8	7.6	37.0	14
56	1KS22EC058	MADHU HAROMUCHADI	15	12	3	30	10	13	23	2	15	17	10	2	2	2	2	2	4.6	4.7	4.7	4.5	4.8	8.9	8.5	8.7	8.8	9.1	44.0	39
57	1KS22EC059	MALLEMPUTA SUSHMITHA	11	11	0	22	3	10	13	4	7	11	10	2	2	2	2	2	3.8	3.8	3.8	3.8	3.9	7.5	7.5	7.0	7.9	7.0	37.0	23
58	1KS22EC060	MALLIKARJUNA SWAMY N	6	13	4	23	5	7	12	4	16	20	9	2	1	2	2	2	3.6	3.6	3.5	3.7	3.7	6.5	6.6	6.9	7.4	8.1	36.0	19
59	1KS22EC061	MANASA CHOWDARY	12	14	7	33	10	14	24	5	17	22	10	2	2	2	2	2	4.9	4.9	4.9	4.9	5	8.7	9.0	9.5	9.8	9.6	47.0	37
60	1KS22EC062	MANOJKUMAR N	4	8	4	16	9	8	17	5	19	24	9	1	2	2	2	2	3.6	3.8	3.7	3.8	3.8	5.2	7.0	7.7	7.8	8.7	37.0	24
61	1KS22EC063	MEGHANA S R	19	16	8	43	6	14	20	5	20	25	10	2	2	2	2	2	4.7	5	5	5	5	9.6	9.4	10.0	9.9	10.0	49.0	24
62	1KS22EC064	MEGHARAJ C M	11	10	7	28	9	11	20	5	20	25	10	2	2	2	2	2	4.2	4.2	4.2	4.2	4.2	7.9	7.7	8.6	8.6	9.2	42.0	28
63	1KS22EC065	MOHAMMED TAHA	19	19	3	41	10	13	23	2	11	13	9	1	2	2	2	2	4.7	4.8	4.7	4.6	4.8	8.6	9.7	8.7	8.9	8.5	45.0	34
64	1KS22EC066	MONIKA H N	9	11	8	28	8	12	20	5	5	10	10	2	2	2	2	2	4.4	4.5	4.7	4.6	4.8	7.8	8.2	9.1	9.2	7.6	42.0	27
65	1KS22EC067	MONISHA B N	17	18	7	42	10	15	25	5	20	25	10	2	2	2	2	2	4.9	5	5	5	5	9.5	9.7	9.6	10.0	10.0	49.0	39
66	1KS22EC068	NALLANI HEMA	7	8	6	21	7	10	17	2	12	14	10	2	2	2	2	2	4	4.1	4.1	4.1	4.1	7.1	7.3	8.1	7.9	7.0	38.0	18
67	1KS22EC069	NEHA M	8	6	0	14	10	12	22	4	9	13	10	2	2	2	2	2	4.5	4.5	4.4	4.4	4.6	7.7	7.4	7.9	8.8	8.0	40.0	28
68	1KS22EC070	NISARGA M	14	13	6	33	5	20	25	5	20	25	10	2	2	2	2	2	4.5	4.5	4.6	4.6	4.6	8.6	8.5	8.3	10.4	9.6	46.0	35
69	1KS22EC071	NITHYASHREE V L	14	11	9	34	5	9	14	5	12	17	10	2	2	2	2	2	4.2	4.2	4.3	4.2	4.3	8.3	7.9	8.4	8.3	8.1	41.0	30
70	1KS22EC073	POOJA V	15	16	9	40	10	9	19	5	18	23	10	2	2	2	2	2	4.9	5	4.9	4.8	4.8	9.2	9.4	9.8	8.9	9.5	47.0	34
71	1KS22EC074	PRAJWAL P	18	19	8	45	9	9	18	0	16	16	10	2	2	2	2	2	4.9	4.9	5	5	5	9.6	9.8	9.6	8.4	9.4	47.0	36
72	1KS22EC075	PRANAV RAJATH	12	4	6	22	8	5	13	0	12	12	9	2	1	2	2	2	4.7	4.6	4.6	4.7	4.1	8.5	7.0	8.7	7.5	7.9	40.0	36
73	1KS22EC076	PREKSHITHA S	10	6	6	22	9	11	20	2	11	13	10	2	2	2	2	2	3.6	3.6	3.4	3.5	2.9	7.1	6.5	7.7	7.5	6.6	36.0	32
74	1KS22EC077	RACHANA JAGANNATH	18	10	2	30	9	10	19	3	9	12	10	2	2	2	2	2	4.3	4.5	4.3	4.6	3.9	9.0	8.0	8.0	9.0	7.3	42.0	19
75	1KS22EC078	RAGHU H M	14	11	4	29	10	13	23	5	17	22	10	2	2	2	2	2	4.9	4.9	4.9	5	4.8	9.0	8.6	9.0	9.7	10.0	47.0	26
76	1KS22EC079	RAKSHITA M B	2	8		10	4	13	17	2	8	10	10	2	2	2	2	2	4.5	4.6	4.6	4.6	3.9	6.8	7.8	7.2	8.9	7.1	38.0	24
77	1KS22EC080	RANJITH GOWDA K	9	6	4	19	5	12	17	3	10	13	10	2	2	2	2	2	4.3	4.3	4.3	4.4	3.8	7.7	7.2	7.7	8.7	7.3	39.0	29
78	1KS22EC081	ROHITH D YADAV	15	20	5	40	3	11	14	4	9	13	10	2	2	2	2	2	4.5	4.5	4.6	4.2	4.2	8.8	9.5	7.8	8.5	7.6	43.0	31
79	1KS22EC082	ROHITH M	17	18	5	40	7	13	20	5	14	19	10	2	2	2	2	2	5	4.7	4.9	5	4.5	9.6	9.4	8.7	9.7	8.6	46.0	39
80	1KS22EC083	SACHIN BASAPPA BARANNAVAR	16	12	5	33	9	10	19	2	12	14	10	2	2	2	2	2	4.3	4.5	4.2	4.6	4	8.7	8.3	8.3	8.4	7.8	42.0	27
81	1KS22EC084	SAHANA K R	11	12	3	26	9	7	16	4	11	15	10	2	2	2	2	2	4.1	4.1	4.1	4.2	3.8	7.8	7.9	7.9	7.9	8.0	40.0	22
82	1KS22EC085	SAHANA N R	4	15	10	29	3	6	9	5	6	11	10	2	2	2	2	2	4.3	4.6	4.4	4.3	4.8	6.9	8.9	8.4	8.0	7.7	40.0	35
83	1KS22EC086	SAHANA T BASANAGOUDRA	16	9	4	29	4	12	16	1	11	12	10	2	2	2	2	2	4.3	4.4	4.2	4.5	3.9	8.7	7.8	7.4	8.5	7.6	40.0	29
84	1KS22EC087	SARIKA S	9	4	6	19	4	4	8	2	10	12	10	2	2	2	2	2	4.3	4.2	4.2	4.3	3.7	7.7	6.8	7.7	7.2	7.2	37.0	29
85	1KS22EC088	SHALINI S	14	19	4	37	5	10	15	2	4	6	10	2	2	2	2	2	4.4	4.5	4.5	4.4	4.1	8.5	9.4	7.9	8.2	6.7	41.0	37
86	1KS22EC089	SHASHANK C	9	7	5	21	5	9	14	4	14	18	10	2	2	2	2	2	4.5	4.6	4.5	4.5	4.1	7.0	7.7	8.0	8.5	8.2	40.0	18
87	1KS22EC090	SHILPA T R	18	13	9	40	5	12	17	4	15	19	10	2	2	2	2	2	4.8	5	5	4.9	4.5	9.5	9.0	9.1	9.3	8.8	46.0	30

88	1KS22EC091	SHRAVANI G V	18	14	9	41	10	13	23	5	15	20	10	2	2	2	2	2	4.3	4.6	4.4	4.6	4.8	9.0	8.7	9.3	9.3	9.1	46.0	34
89	1KS22EC092	SHREE HARSHITHA S	12	14	9	35	2	7	9	2	13	15	10	2	2	2	2	2	4.2	4.2	4.2	4.2	3.9	8.0	8.3	7.9	7.6	7.9	40.0	28
90	1KS22EC093	SIDDHARTH SHARMA	13	15	2	30	9		19	5	19	24	10	2	2	2	2	2	4.4	4.6	4.5	4.4	4.6	8.4	8.9	8.2	8.7	9.5	44.0	33
91	1KS22EC094	SINCHANA S S	4	13	8	25	7	9	16	3	7	10	10	2	2	2	2	2	4.1	4.2	4.4	4.3	4.4	6.7	8.2	8.0	8.1	7.5	39.0	27
92	1KS22EC095	SNEHA	11	17	9	37	8	14	22	4	18	22	10	2	2	2	2	2	4.8	4.9	4.8	5	4.8	8.5	9.5	9.4	9.7	9.5	47.0	28
93	1KS22EC096	SOUMYASHREE F SARAF	9	5		14	4	7	11	2	7	9	10	2	2	2	2	2	4.4	4.3	4.3	4.2	4	7.8	7.1	6.9	7.6	7.1	37.0	35
94	1KS22EC097	SOWJANYA RAI	14	20	8	42	5	9	14	5	17	22	10	2	2	2	2	2	4.4	4.3	4.2	4.1	4.5	8.5	9.3	8.2	8.2	9.1	44.0	32
95	1KS22EC098	SPOORTHY B	14	18	4	36	10	12	22	3	13	16	10	2	2	2	2	2	4.4	4.4	4.4	4.4	4.6	8.5	9.1	8.5	8.7	8.6	44.0	25
96	1KS22EC099	SRUJAN H G	10	12	3	25	9	7	16	1	9	10	10	2	2	2	2	2	4.2	4.3	4.3	4.4	4.6	7.7	8.1	8.1	7.6	8.0	40.0	25
97	1KS22EC100	SRUJAN KARANTH N	15	18	3	36	7	13	20	5	14	19	10	2	2	2	2	2	4.7	4.7	4.7	4.5	4.9	9.0	9.4	9.0	9.2	9.0	46.0	21
98	1KS22EC101	SULAGNA MONDAL	16	20	8	44	7	13	20	4	17	21	10	2	2	2	2	2	4.6	4.7	4.6	4.7	4.9	9.0	9.7	8.9	9.3	9.5	47.0	36
99	1KS22EC102	SUMANJALI K	19	20	7	46	10	13	23	5	19	24	10	2	2	2	2	2	4.6	4.7	4.6	4.8	4.6	9.5	9.7	9.0	9.0	9.5	47.0	35
100	1KS22EC103	SUNITA SHIVASHANKAR	18	10	6	34	5	10	15	3	9	12	10	2	2	2	2	2	4.2	4.2	4.2	4.2	4.7	8.9	7.7	7.9	9.0	8.1	42.0	29
101	1KS22EC104	SURYA R V	7	5		12	2	8	10	7	5	12	10	2	2	2	2	2	3.8	3.7	3.6	3.7	4.1	6.9	7.0	5.9	8.0	6.9	35.0	14
102	1KS22EC105	SWATHI S	7	4	9	20	4	6	10	1	3	4	7	2	1	2	1	1	3.4	3.2	3.4	3.1	3.4	6.5	4.8	7.4	6.0	4.9	30.0	2
103	1KS22EC106	TEJASWINI R	12	7	7	26	5	4	9	3	14	17	10	2	2	2	2	2	4.4	4.4	4.5	4.3	4.7	8.2	7.5	8.3	7.4	8.0	40.0	19
104	1KS22EC107	THANUSHREE M K	6	6		12	2	9	11	1	12	13	10	2	2	2	2	2	4.1	4	4	3.9	4.2	7.0	6.9	7.0	7.4	8.0	37.0	32
105	1KS22EC108	TIRUMALA GANESH BHARADWAJ SHARMA	16	7		23	5	5	10	0	2	2	10	2	2	2	2	2	4.2	4.2	4.3	4.2	4.6	8.6	7.3	8.0	7.0	6.9	38.0	22
106	1KS22EC109	UMME SARA	17	18	10	45	9	14	23	5	20	25	10	2	2	2	2	2	4.8	4.8	5	4.9	5	9.4	9.5	9.9	9.8	10.0	49.0	37
107	1KS22EC110	V LIKHITH	17	14	6	37	1	8	9	2	5	7	10	2	2	2	2	2	4.5	4.3	4.6	4.4	4.7	9.1	8.4	7.7	7.9	7.5	41.0	23
108	1KS22EC111	VARDHAN GOWDA K N	14	12	5	31	9	7	16	4	7	11	10	2	2	2	2	2	4.4	4.3	4.2	4.1	4.4	8.5	8.1	8.3	7.8	7.5	41.0	37
109	1KS22EC112	VARSHA B C	12	11	4	27	7	14	21	4	3	7	10	2	2	2	2	2	4	4.1	4.3	4	4	7.8	7.8	8.0	8.7	6.5	39.0	42
110	1KS22EC113	VARSHINI S	15	15	6	36	9	11	20	5	13	18	10	2	2	2	2	2	4.6	4.7	4.5	4.7	4.8	8.9	9.0	8.8	9.1	8.8	45.0	32
111	1KS22EC114	VARUN	4	15	4	23	3	14	17	4	14	18	10	2	2	2	2	2	5	4.9	4.9	4.8	4.9	7.6	9.2	8.0	9.5	9.0	44.0	31
112	1KS22EC115	VARUN RAYAPATI R	11	8		19	6	12	18	3	13	16	10	2	2	2	2	2	4.4	4.3	4.4	4.4	4.4	8.1	7.5	7.3	8.7	8.4	40.0	26
113	1KS22EC116	VEDASHREE M	9	20	10	39	7	10	17	5	18	23	10	2	2	2	2	2	4.9	5	4.8	4.9	5	8.3	10.0	9.4	9.2	9.7	47.0	28
114	1KS22EC117	VIDYASHREE H	8	12	4	24	8	11	19		15	15	10	2	2	2	2	2	4.2	4.2	4.2	4.4	4.2	7.4	8.0	8.0	8.1	8.5	40.0	23
115	1KS22EC118	VIJAYKUMAR SHANMUKHAYYA	7	4		11	9	5	14	4	8	12	10	2	2	2	2	2	3.7	3.5	3.6	3.5	3.6	6.8	6.1	7.0	6.9	6.8	34.0	27
116	1KS22EC119	VIKAS K S	13	18	4	35	9	12	21	4	20	24	10	2	2	2	2	2	4.8	5	4.9	5	5	8.8	9.7	8.9	9.4	10.0	47.0	31
117	1KS22EC120	VISHWANATH B S	16	10	4	30	6	12	18	2	11	13	9	2	2	1	2	2	3.6	3.6	3.6	3.6	3.8	8.0	7.1	6.1	7.7	7.5	37.0	32
118	1KS22EC121	VISHWANATH VEERAPUR	18	5		23	5	1	6	4	9	13	10	2	2	2	2	2	4.4	4.3	4.4	4.3	4.2	9.1	7.1	8.0	7.1	7.6	39.0	35
119	1KS22EC122	VISHWAS M K	14	15	8	37	5	6	11	3	10	13	10	2	2	2	2	2	4.4	4.4	4.2	4.3	4.3	8.5	8.7	9.0	7.7	7.8	42.0	30
120	1KS22EC123	VIVEK M S	16	8	3	27	2	5	7	4	13	17	10	2	2	2	2	2	4.3	4.2	4.3	4.3	4.4	8.7	7.4	7.1	7.7	8.4	40.0	35
121	1KS22EC124	VIVEK RAJ B	15	17		32	5	8	13	5	11	16	10	2	2	2	2	2	4.8	4.9	5	4.9	4.9	10.0	9.5	7.8	8.9	8.6	45.0	34
122	1KS22EC125	YASHAVANTHA S	5	3	8	16	4	10	14	4	10	14	6	1	2	1	1	1	3.8	3.8	3.8	3.8	3.4	5.6	6.3	6.6	6.9	5.9	32.0	20
123	1KS22EC126	YASHWANTH P V	10			10		9	9	4	12	16	10	2	2	2	2	2	3.8	4	4	4.2	4	7.3	6.0	6.0	8.2	7.8	36.0	18
124	1KS23EC400	BHAVAN M	15	5	10	30	1	4	5	2	0	2	10	2	2	2	2	2	4	4	4	4	4.1	8.3	6.8	7.7	6.9	6.1	36.0	21
125	1KS23EC401	CHETHAN B L	14	9		23	5	3	8	2	5	7	10	2	2	2	2	2	3.9	4	4	4.2	4.2	8.0	7.4	6.8	7.0	7.0	36.0	25
126	1KS23EC402	CHINMAYI R	18	6		24	6	4	10			0	10	2	2	2	2	2	4.4	4.4	4.4	4.4	4.4	9.1	7.3	7.3	7.0	6.4	38.0	13
127	1KS23EC403	DEEKSHITH A	14	13		27	1	1	2	2	3	5	6	2	1	1	1	1	3.6	3.5	3.3	3.6	3.6	7.7	6.5	4.5	5.1	5.1	29.0	18
128	1KS23EC404	HARISH N	9	8	6	23	4	4	8	2	5	7	10	2	2	2	2	2	3.8	3.6	3.7	3.8	3.4	7.2	6.8	7.2	6.7	7.0	35.0	25
129	1KS23EC405	HARSHITH M K	10	5		15	1	6	7	4	10	14	10	2	2	2	2	2	3.4	3.7	3.8	3.8	3.8	6.9	6.5	6.0	8.0	8.0	36.0	26
130	1KS23EC406	MANOJ R	16	6	6	28	4	4	8	1	0	1	10	2	2	2	2	2	4.2	4.2	4.2	4.2	4.4	8.6	7.1	7.7	7.0	6.4	37.0	25
131	1KS23EC408	NIKHIL M S	14	2	8	24	5	5	10	0		0	10	2	2	2	2	2	4	4.2	4.1	4	4.2	8.1	6.5	8.1	6.8	7.0	37.0	31
132	1KS23EC409	VIJAY D S	12	8	0	20	5	9	14	5	2	7	10	2	2	2	2	2	4.3	4.4	4.3	4.1	4.4	8.1	7.6	7.1	9.0	6.7	39.0	19
133	1KS23EC410	VIKAS GOWDA B S	17	4		21	5	5	10	3	2	5	10	2	2	2	2	2	4	3.8	3.8	3.8	3.9	8.6	6.4	6.6	7.0	6.2	35.0	22
																		60% of Maximum marks (X)					6	6	6	6	6	30	30
																		No. of students above X					129	132	128	131	128	132	59

CO	CIE	SEE	Direct Attainment in %	Direct Attainment in Level	Indirect ttainment	Final Attainment
CO1	96.99	44.36	70.6767	3	3	3.00
CO2	99.25	44.36	71.80	3	3	3.00
CO3	96.24	44.36	70.3008	3	3	3.00
CO4	98.50	44.36	71.43	3	3	3.00
CO5	96.24	44.36	70.30	3	3	3.00
AVERAG						03.00

Total number of students (Y)	133	133	133	133	133	133	133
CO Percentage	96.99	99.25	96.24	98.50	96.24	99.25	44.36
CO level	03	03	03	03	03	03	00

Donot delete any DIV/0 values in the cells,
after entering marks, they will automatically get updated.

Co-Po Mapping Table														
CO'S	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PS01	PSO2
CO1	3	3	3	_	3	_	_	2	2	3	_	2	3	3
CO2	3	3	3	2	3	_	_	2	2	3	_	2	3	3
CO3	3	3	3	_	3	_	_	2	2	3	_	2	3	3
CO4	3	3	3	_	3	_	_	2	2	3	_	2	3	3
CO5	3	3	3	2	3	_	_	2	2	3	_	2	3	3
AVG	3.00	3.00	3.00	2.00	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00

PO Attainment	CO Attainment	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PS01	PSO2
CO1	3.00	3.00	3.00	3.00	_	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00
CO2	3.00	3.00	3.00	3.00	2.00	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00
CO3	3.00	3.00	3.00	3.00	_	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00
CO4	3.00	3.00	3.00	3.00	_	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00
CO5	3.00	3.00	3.00	3.00	2.00	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00
AVERAGE		3.00	3.00	3.00	2.00	3.00	_	_	2.00	2.00	3.00	_	2.00	3.00	3.00