SAHANA SHARMA M
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Profile:
Pursuing Ph.D. (AI and Networking area) under VTU (Visvesvaraya Technological University), registered in the year 2017 and have completed comprehensive viva.

A student focused Assistant Professor with 6 years of experience in delivering and implementing engineering curriculum. Skilled at explaining complex concepts in a simple form with real time examples. Looking forward to contributing my knowledge and skills in an institution that offers opportunity for career progression.

Currently teaching Computer Science and Information Technology for International Baccalaureate Diploma Program with 3 years of experience.

Education Summary

Degree and Year	*Institution*	*Percentage*	*Specialization*	*University*
Pursuing Ph.D. Waiting for open seminar.	Research Centere: NMAMIT, Nitte, Karkala, Udupi		Artificial Intelligence and Networking	VTU, Belgaum, Karnataka
MTech 2011-2013	T.John Institute of Technology, Bengaluru-76, Karnataka.	71%	VLSI Design and Embedded Systems.	VTU, Belgaum, Karnataka.
BE 1995-1999.	Siddaganga Institute of Technology, Tumakuru, Karnataka.	67%	Electronics and Instrumentation	Bangalore University, Karnataka.
Intermediate 1993-1995.	Vijaya College, Mulki, Mangalore, Karnataka	64%	PCMB	Karnataka State Board
SSLC- 1993	B.E.M High School, Kasaragod, Kerala.	83%		Kerala State Board

Work History

August 2019 till date IBDP Faculty Computer Science	***Subject Handled:*** Computer Science and Information Technology. Theory: Computer Organization, Computational Thinking, Algorithms and Pseudocodes, Data Structures, Computer Networks, RDBMS. Lab: Web Programming Lab (Java script), Graphics and Illustrator (Adobe), Database (MS Access).
August 2013 till August 2019 Assistant Professor Acharya Patashala College of Engineering (APSCE). Kanakapura Road, Bengaluru, Karnataka.	***Subject Handled:*** 1. CCN (Computer Communication and Networking) handled 3 times 2. ADE (Analog and Digital Electronics) for CSE handled 3 times. 3. OFC (Optical Fiber Communication) handled 2 times. 4. CMOS VLSI Design handled once. 5. LIC (Linear Integrated Circuits) handled two times. 6. Microelectronics and Circuits (MEC) handled 3 times 7. PCS (Principles of Communication Systems) handled once. 8. Basic Electricals handled 8 times. ***Laboratory Subjects:*** 1. CCN (In-charge) lab 3 times. 2. ADE (In-charge) lab 3 times for CSE. 3. VLSI lab two times. 4. Electronics Circuits Lab (In-charge) two times. 5. Communication Lab two times. 6. DSP Lab (In-charge) handled once. 7. HDL Lab (In-charge) handled two times. 8. Digital Electronics Lab handled two times. 9. Basic Electrical Lab (In-charge) handled once. ***Subject handled for M.Tech*** Advances in VLSI for M.Tech handled twice.
Jan 2000 July 2001 Faculty Manipal Institute of Computer Education (MICE).	*Subject Handled*: C and C++ Programming. Performed various administrative functions including filing paperwork, delivering mail, and sorting mail.

Technical Proficiency

Electronic Design Automation (EDA) Tools.	Cadence, Mentor Graphics, Xilinx ISE.
Simulation Tools	Matlab, Network Simulator NS2
Computer Programming Languages	Python, Java script, VHDL, VERILOG, C, C++
Basic Computer Skills	Microsoft Word, Excel, Powerpoint, Graphic design tools, Adobe Illustrator, Adobe Animate CC and Photoshop.

Paper Publications/Presentations

1. Published a paper entitled "Recovery schemes for various challenges in Elastic Optical Networks" in International Research Journal Of Modernization In Engineering Technology And Science (IRJMETS), Volume 4, Issue 02, February 2022.
e-ISSN: 2582-5208, Ref: IRJMETS/Certificate/Volume 4/Issue 02/40200005266.

2. Presented the paper titled "Design and Implementation of Direct Digital Synthesizer for 5G Systems" at the International Conference on Signal Processing, Communication and Embedded Control (ICSPCEC-19) held at APSCE from 3rd – 4th May 2019.

3. Participated with the paper titled "Implementation of Secure test wrapper Design Against Scan based Attacks" in National Conference on "Communication & Image Processing-NCCIP-13", held at T.John Institute of Technology on Aug 7th 2013.

Certified Courses/ Training	Undergone BSNL Internship in Advanced Digital Switching Systems & Optical Fiber Communication at RTTC, Mysuru from 8-01-2018 to 13-01-2018.
	Participated in Summer School in Optics and Photonics (SOAP) organized by Applied Photonics Initiative, Indian Institute of Science (IISc), Bengaluru from 25th July to 28th July 2018.
Workshops/ FDP	Five day Faculty Development program on "Graphical Programming, Data Acquisition and Hardware Programming using NI LabVIEW" held at DSATM, Bengaluru from 28th June to 2nd July 2019.
	Faculty development program on "VLSI Design and Methodology" held at APSCE, Bengaluru between 10th and 11th March 2016.
	Five day Faculty Development program on "Research Opportunities in Signal Processing and Image Processing" held at Jyothy Institute of Technology, Bengaluru, from 18th to 23rd January 2016.

	Twelve-day workshop for faculties on "Signals and Systems" under ISTE, conducted by IIT Kharagpur and IIT Bombay held at Amrita School of Engineering, Bengaluru from Jan 2nd to Jan 12th 2014.
	Two-day workshop on low power Embedded Systems using MSP430 organized by T John Institute of Technology, 2013, Bengaluru.

Other Curriculum/ Co-curriculum Responsibilities:

College level responsibilities:

- Lead of organizing committee for Drishti Online Contest under Texas Instruments India University Program.
- Conducted sessions on Communication Skills as part of orientation program for first year BE students.
- Escorted students for NSS camp as a teacher in charge for 3 days.
- Member of cultural committee.
- Member of exam committee.
- Member of academic monitoring committee.

Department level responsibilities

- Timetable coordinator for 3 times
- Mentor coordinator for 4 times
- Test coordinator for 3 times.
- Seminar coordinator for one time.
- Project coordinator for one time
- Cultural coordinator for two times
- Compered and handled various sessions for National and International conferences held in the college

Personal skills

- Comprehensive problem-solving abilities with international mindedness.
- Good verbal and written communication skills.
- Ability to deal with people diplomatically.
- Willingness to learn.
- Team facilitator and hard worker.

Key Projects:

Project: Inventory Management System	**Duration:** 1/10/2000 to 5/11/2000
Organization: NACE(National Academy Of Computer Education), Mangalore	
Project description: The project was based on "Inventory Management System", processing the transaction of inventories concerning soap manufacturing unit. The module was designed using VB6.0. The project is GUI based and user friendly, above all consisting of all prerequisites of basic inventory management system. The module has the provision for adding new records, deleting the records after checking the conditions, searching the records and finally to print the report and the sale bill.	
Software used: VB6.0, MS-Access, Windows98	

BE Project

Project: DSP based pipeline flow controller.	**College:** SIT (Siddaganga Institute of Technology), Tumkur.
DSP Kit Provider: Texas Instruments, Bangalore	
Project description: The project was to control the water flow in a pipeline. Of the various techniques available to sense the flow rate, combination of head type meters (orifice) and solid state differential pressure transducers (DTP) offers the best solutions. Hence this scheme was used. The water flow in a pipeline is controlled accurately and the system was built around DSP-TMS 320 C50, a very fast and reliable processor. The DTP's output voltage, a linear function of flow rate, is suitably signal conditioned. This voltage was processed by processor TMS320 C50(Texas Instruments) with the aid of an Analog Interface Circuit (AIC). The DSP was programmed to find error signal as the difference between user set flow rate and the actual flow rate. It was further programmed to execute a proportional controller algorithm thus adjusting the flow rate to the desired value.	

M.Tech Project

Project: Implementation of Secure Test wrapper design against scan-based attacks.	**College:** T.John Institute of Technology, Bangalore 2012-2013
Project description: The project was to design a secure test wrapper for IP cores. The project presents a secure DfT (Design for Testability) design, secure test wrapper (STW) which is fully compatible with IEEE 1500 standard. STW protects internal scan chains, primary inputs and outputs, which may contain critical information such as encryption key during the system operation. Area overhead of the STW is reduced by re using flip-flops in the wrapper boundary cells as the LFSR (Linear Feedback Shift Register) to generate the golden key. The proposed system provides protection against both scan-based controllability and observability attacks. The design has been implemented on Spartan 3s400 with efficient device utilization.	
Simulation of the project has been carried out using Modelsim software (Version 6.2c). Verilog code is used to generate the circuit using Xilinx synthesis tool.	

Personal Details

Date of Birth	18-04-1978
Nationality	Indian
Marital Status	Married
Co-curricular Activities	Carnatic Music, Rajya Puraskar awardee for Scouts and Guides.

Declaration

I hereby declare that the above-mentioned information is true to the best of my knowledge and belief.

Date: 16-03-2022
Place: Bangalore

(SAHANA SHARMA M)