| K.S.INSTITUTE OF TECHNOLOGY | | | | |
|---|---|---|---|---|
| DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG. | | | | |
| INTERNSHIP DETAILS | | | | |
| ACADEMIC YEAR 2024-25 | | | | |
| **Sl. No.** | **USN** | **NAME OF THE STUDENT** | **Internship Domain** | **Internship Project** |
| **1** | **1KS21EC001** | **AADHYA B N** | **VLSI** | **Design of an 32 bit floating point subtraction using Verilog HDL** |
| **2** | **1KS21EC002** | **ABHIJITH R** | **VLSI** | **3 to 9 decoder using the Verilog HDL** |
| **3** | **1KS21EC003** | **ABHISHEK H C** | **VLSI** | **8:1 Mux using Verilog HDL** |
| **4** | **1KS21EC004** | **ABHISHEK T S** | **AIML** | **Automated model ensemble techniques for improved accuracy** |
| **5** | **1KS21EC005** | **AISHWARYA A** | **ALQWIP** | **Business Analyst** |
| **6** | **1KS21EC006** | **AKSHAY C** | **VLSI** | **To design a four bit binary to grey using Verilog HDL** |
| **7** | **1KS21EC007** | **AKSHAY M S** | **AIML** | **Cognitive customer insights with watson AI** |
| **8** | **1KS21EC008** | **ANAGHA PRAKASH** | **VLSI** | **8:1 Mux using Verilog HDL** |
| **9** | **1KS21EC009** | **ANIRUDHA R BHAT** | **VLSI** | **8:1 mux using Verilog HDL** |
| **10** | **1KS21EC010** | **ARCHANA G M** | **VLSI** | **8 bit ripple carry adder using Veilog** |
| **11** | **1KS21EC011** | **ARCHANA M** | **VLSI** | **Design of an 8:1 mux using verilog HDL** |
| **12** | **1KS21EC013** | **ASHCHARYA N B** | **VLSI** | **4 bit up/down coumter using verilog HDL** |
| **13** | **1KS21EC014** | **ASHWIN S R** | **VLSI** | **Design 8:1 subtractor circuit using verilog HDL** |

| Sl. No. | USN | NAME OF THE STUDENT | Internship Domain | Internship Project |
|---|---|---|---|---|
| 14 | 1KS21EC015 | B N JEEVAN | AI Devops Engineer | Real time social media analyticas pipeline: building a robust data processing framework |
| 15 | 1KS21EC017 | B S BHARGAV | AI Devops Engineer | Establishing a CI/CD pipeline for automated deployments |
| 16 | 1KS21EC018 | BHAVYA K | VLSI | Design an 8bit shifter which can shift left/right by n bits based on the given inputs using Verilog HDL |
| 17 | 1KS21EC019 | BHUVANA H | VLSI | Design an 8-bit magnitude comparator using verilog HDL |
| 18 | 1KS21EC020 | BINDUSHREE S | VLSI | Design a 4 bit up/down counter using Verilog HDL |
| 19 | 1KS21EC021 | CHINTAN D S | AI Devops Engineer | E-Commerce Website |
| 20 | 1KS21EC023 | CHIRANTH V V | VLSI | Design a sequence detector 110 using Verilog HDL |
| 21 | 1KS21EC024 | DAGGUPATI CHARITHA | VLSI | 8 bit ripple carry adder using verilog |
| 22 | 1KS21EC025 | DAMINI S | VLSI | Design 32 bit floating polint subtraction using IEEE 754 representation |
| 23 | 1KS21EC026 | DEEKSHA H K | VLSI | 32 bit floating point multiplication based on IEEE 754 representation using verilog HDL |
| 24 | 1KS21EC027 | DEEPIKA D | VLSI | Design, verification and implementation of sequence detector 110 using Verilog HDL |
| 25 | 1KS21EC028 | GAGAN V | VLSI | Design 4 bit binary to grey code converter using Verilog HDL |
| 26 | 1KS21EC029 | GAGANA SINDHU N | VLSI | To design a 4-bit up/down counter |
| 27 | 1KS21EC031 | GURUSHANKAR A M | VLSI | Design 3 to 8 Decoder using Verilog HDL |

| Sl. No. | USN | NAME OF THE STUDENT | Internship Domain | Internship Project |
|---|---|---|---|---|
| 28 | 1KS21EC032 | HARINI L | VLSI | Design 4 bit binary to grey code converter using Verilog HDL |
| 29 | 1KS21EC033 | HEMANTH D R | VLSI | Design 8:1 mux verilog HDL |
| 30 | 1KS21EC035 | KAMBHAMPATI VIVEK | VLSI | Design 8-bit subractor using the verilog HDL |
| 31 | 1KS21EC036 | KARAN S | VLSI | Design of an 4-bit up/down counter using verilog system VHDL |
| 32 | 1KS21EC037 | KEERTHANA S | VLSI | Design 8-bit subractor using the verilog HDL |
| 33 | 1KS21EC038 | KOMALA N | Mphasis | Trade file load Management system |
| 34 | 1KS21EC039 | KUSHAL GOWDA U | AIML | Contextual language understanding with transformermodels |
| 35 | 1KS21EC040 | KUSUMA M S | VLSI | To design a 4-bit adder cum subtractor |
| 36 | 1KS21EC041 | LIKITHA L | VLSI | To design a four bit adder cum subtactor using Verilog |
| 37 | 1KS21EC042 | LOHIT S HOOLAGERI | AI Devops Engineer | Congnitive customer insights with watson AI |
| 38 | 1KS21EC043 | LOHITH B | AI Devops Engineer | Real time chat application |
| 39 | 1KS21EC044 | LOHITH S | AI Devops Engineer | Conextual language understanding with transformer models |
| 40 | 1KS21EC045 | MANOJ T V | AIML | Congnitive customer insights with watson AI |
| 41 | 1KS21EC046 | MEGHANA N | VLSI | Design a 4 bit binary to gray converter using Verilog HDL |
| 42 | 1KS21EC047 | MISBA M | AI Devops Engineer | E-Commerce Website |
| 43 | 1KS21EC048 | MITHUN C | VLSI | Design an 8 bit magnitude comparator using Verilog HDL |

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|---|---|---|---|---|
| 44 | 1KS21EC049 | MONISHA D | AI Devops Engineer | Adipting multicloud statergy with Docker and Kubernets |
| 45 | 1KS21EC050 | MUTTHULURU SAI HIMAJA | AIML | Automated model ensemble techniques for improved accuracy |
| 46 | 1KS21EC051 | NANDAN K | VLSI | Design 8-bit subractor using the verilog HDL |
| 47 | 1KS21EC053 | NARAHARI N JOSHI | VLSI | Design Vewrification and implementation of 110 sequence detector |
| 48 | 1KS21EC054 | NAVEEN S | VLSI | To design a four bit adder cum subtactor using Verilog |
| 49 | 1KS21EC055 | NAYANA J | VLSI | Design of an 32 bit floating point subtraction using Verilog HDL |
| 50 | 1KS21EC056 | NAYANA S | AI Devops Engineer | E-Commerce Website |
| 51 | 1KS21EC058 | OMKAR N BHUJARKAR | AI Devops Engineer | Tracling the effectiveness of automation in DEVOPS uing multi-tier application |
| 52 | 1KS21EC059 | PAVAN M PAI | VLSI | Design an 8-bit magnitude comparator using verilog HDL |
| 53 | 1KS21EC060 | POLURU MANJUNATH | VLSI | Detecting the sequence 110 from the inputs trained using verilog HDL |
| 54 | 1KS21EC061 | POOJA R | VLSI | 32 bit floating point addition |
| 55 | 1KS22EC400 | ADITHYA D | VLSI | Designing a four bit priority encoder using verilog HDL |
| 56 | 1KS22EC401 | APOORVA B | AIML | Contextual language understanding with transformermodels |

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|---|---|---|---|---|
| 57 | 1KS22EC402 | B SREEPADREDDIH BULLANGOUDAR | VLSI | Sequence detector 110 using verilog HDL |
| 58 | 1KS22EC403 | CHAITRA N | VLSI | Design of an 8bit ripple carry adder using Verilog HDL |
| 59 | 1KS22EC404 | GONUGUNTLA SHRUJANA | VLSI | Design a eight bit shifter which can shift left/right by n bits based on the given inputs using verilog HDL |
| 60 | 1KS22EC405 | HEMA K | VLSI | Design vewrification and implementation of 1:8 mux using verilog HDL |
| 61 | 1KS22EC406 | PAVANGOWDAH P | VlSI | Design of an 8 bit ripple carry adder using verilog HDL |
| 62 | 1KS21EC062 | PRAJWAL D | AIML | Real time social media analytics pipeline building robust dataprocessing framework |
| 63 | 1KS21EC063 | PRAJWAL G V | AI Devops Engineer | Real time chat application |
| 64 | 1KS21EC064 | PRAJWAL H S | VLSI | Design 3 to 8 decoder using verilog HDL |
| 65 | 1KS21EC065 | PRAJWAL R | VLSI | Design an 8 bit ripple carry adder using ine bit full addrer with verilog HDL |
| 66 | 1KS21EC066 | PRATHAM R SHANBHAG | VLSI | Designn an 8 bit shifter which can shift left/right by n bits based on given inputs using verilog HDL |
| 67 | 1KS21EC067 | PRAYAG SINGH S | VLSI | Design 32bit floating point multiplication bbased on IEEE 754 representation using Verilog HDL |
| 68 | 1KS21EC068 | PREETHAM M | VLSI | Design an eight bit ripple carry adder using 1bit full adder using verilog HDL |
| 69 | 1KS21EC069 | PREKSHA S | VLSI | Designing a 32 bit floating adder using Verilog HDL |
| 70 | 1KS21EC070 | PUNITH M | VLSI | 32-Bit flowing point subractor |

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|---|---|---|---|---|
| 71 | 1KS21EC071 | RAGHAVENDRA NARAYAN PUJAR | AIML | Real time social media analytics pipeline building robust dataprocessing framework |
| 72 | 1KS21EC072 | RAKSHITH S | AI Devops Engineer | Real time chat application |
| 73 | 1KS21EC073 | RAKSHITHA M R | VLSI | Design an eight bit ripple carry adder using 1bit full adder using verilog HDL |
| 74 | 1KS21EC074 | RAYADURG JOISH SHRIYA | VLSI | Design 32bit floating point multiplication bbased on IEEE 754 representation using Verilog HDL |
| 75 | 1KS21EC075 | REHAMAN SHARIFF | AI Devops Engineer | E-Commerce Website |
| 76 | 1KS21EC076 | RITESH KUMAR SINHA | VLSI | Design an 8 bit shifter which can shift left/right by n bits based on the given input using Verilog HDL |
| 77 | 1KS21EC077 | RITHIKA M | VLSI | Design of an 4 bit priority encoder using Verilog HDL |
| 78 | 1KS21EC078 | S HARI DHANUSH | VLSI | Design 3 to 8 decoder using verilog HDL |
| 79 | 1KS21EC080 | S SHAJITH ALI | AIML | Automated model ensemble techniques for improved accuracy |
| 80 | 1KS21EC081 | SAGAR G S | AI Devops Engineer | Real time chat application |
| 81 | 1KS21EC082 | SAI RAHUL N | AIML | Contextual language understanding with transformer models |
| 82 | 1KS21EC083 | SAMHITHA PRAKASH | VLSI | Design 3 to 8 decoder using verilog HDL |
| 83 | 1KS21EC084 | SANJANA V | VLSI | Designing a 32 bit floating subtractor using Verilog HDL |
| 84 | 1KS21EC085 | SANJAY G | VLSI | Design a 3 to 8 decoder using Verilog HDL |
| 85 | 1KS21EC086 | SANJAY N | VLSI | Designing a four bit priority encoder using Verilog HDL |
| 86 | 1KS21EC087 | SANJAY P | VLSI | Design 32 bit floating poing multiplication based on IEEE 754 representation uasing the Verilog |

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|---|---|---|---|---|
| 87 | 1KS21EC088 | SATHYAM KUMAR MANDAL S | VLSI | Design an 8 bit magnitutde comparator using Verilog HDL |
| 88 | 1KS21EC089 | SHAIK ARFATH | AI Devops Engineer | E-Commerce Website |
| 89 | 1KS21EC090 | SHASHANK C U | VLSI | Designing a 32 bit bit floating point adder using erilog |
| 90 | 1KS21EC091 | SHREYAS RAGHAVENDRA V | VLSI | Design an 8 bit shifter which can shift left/right by n bits based on the given input using Verilog HDL |
| 91 | 1KS21EC092 | SHWETHA V | VLSI | Design , verification and implementation of 110 sequence detector |
| 92 | 1KS21EC093 | SINDHU M NIMBAL | VLSI | 32-Bit floating point subraction |
| 93 | 1KS21EC095 | SPOORTHY M U | VLSI | 32-floating point multiplication based on IEEE 754 representation |
| 94 | 1KS21EC096 | SRILAKSHMI G | AI Devops Engineer | Establishing CI/CD pipeline for automated Deployment |
| 95 | 1KS21EC097 | SRIPRIYA H G | AI Devops Engineer | Establishing CI/CD pipeline for automated Deployments |
| 96 | 1KS21EC098 | SUMUKH P | VLSI | Designing 32 bit floating point adder using Verilog HDL |
| 97 | 1KS21EC099 | SUNEETHA | VLSI | Design 32 bit floating point multiplication based on IEEE 754 representation using Verilog HDL |
| 98 | 1KS21EC100 | SUNEHA S | VLSI | Design 32 bit floating point adder using Verilog HDL |
| 99 | 1KS21EC101 | SUPREETH A | VLSI | To design a four bit adder/ subtractor using Verilog HDL |
| 100 | 1KS21EC102 | SURABHI K R | VLSI | Design 32 bit floating point multiplication based on IEEE 754 representation using Verilog HDL |
| 101 | 1KS21EC103 | SUSHEN KRISHNAPUR | VLSI | Design an 8 bit shifter which can shift left/right by n bits based on the given input using Verilog HDL |
| 102 | 1KS21EC104 | TARUN M | VLSI | Design of 32 bit floating point subtraction using verilog HDL |

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|---|---|---|---|---|
| 103 | 1KS21EC105 | TEJASHREE N | VLSI | Design, verification and implementation of 110 sequence detector using Verilog HDL |
| 104 | 1KS21EC106 | THARUN K V | VLSI | Design an 8 bit shifter which can shift left/right by n bits based on the given input using Verilog HDL |
| 105 | 1KS21EC107 | THEJAS H V | VLSI | Design an 8 bit magnitutde comparator using Verilog HDL |
| 106 | 1KS21EC108 | THUSHAR CHERIAN | VLSI | Designing a four bit priority encoder using Verilog HDL |
| 107 | 1KS21EC109 | UDAYA KUMAR S R | AIML | Cognitive customer insights with watson AI |
| 108 | 1KS21EC110 | VAISHNAVI B A | AI Devops Engineer | Establishing CI/CD pipeline for automated Deployment |
| 109 | 1KS21EC111 | VARSHA JAYAKUMAR | AI Devops Engineer | E-Commerce Website |
| 110 | 1KS21EC112 | VARSHA S DAVASKAR | VLSI | Design , verification and implementation of an 1:8 demux for 8bit inputs using verilog HDL |
| 111 | 1KS21EC113 | VARSHITH S | VLSI | Design of a 32 bit floating point subtraction using Verilog HDL |
| 112 | 1KS21EC114 | VEERESH K N | AIML | Real time social media analytics pipeline building robust dataprocessing framework |
| 113 | 1KS21EC115 | VIDYA I | VLSI | Design 8 bit magnitude comparator using Verilog HDL |
| 114 | 1KS21EC116 | VIDYA RAWAL D | VLSI | Designing 32 bit floating point adder using Verilog HDL |
| 115 | 1KS21EC117 | VIDYASHREE R | AI Devops Engineer | E-Commerce Website |
| 116 | 1KS21EC118 | VIJAY YADAV R | VLSI | Design an 8 bit shifter which can shift left/right by n bits based on the given input using Verilog HDL |
| 117 | 1KS21EC120 | VYSHAK G R | VLSI | Design of a 32 bit floating point multiplication based IEEE 754 representation using Verilog HDL |
| 118 | 1KS21EC121 | YASHWANTH.M | VLSI | Design of a 32 bit floating point subtraction based on IEEE 754 representation using Verilog HDL |

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|---|---|---|---|---|
| 119 | 1KS22EC407 | PRAJWAL PATIL B S | VLSI | 3 to 8 line decoder using Verilog HDL |
| 120 | 1KS22EC408 | SANGEETHA H M | AI Devops Engineer | E-Commerce Website |
| 121 | 1KS22EC409 | SOUNDARYA S | VLSI | Design, verification and implementation of an 8:1 MUX using Verilog HDL |
| 122 | 1KS22EC410 | SOWMYA A M | VLSI | Design an 8 bit magnitutde comparator using Verilog HDL |
| 123 | 1KS22EC411 | SUDEEP P | VLSI | Design an 8 bit magnitutde comparator using Verilog HDL |