VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering

Scheme of Teaching and Examinations2022

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2023-24)

V SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	HSMS	BEC501	Technological Innovation and Management Entrepreneurship	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
2	IPCC	BEC502	Digital Signal Processing	TD- ECE/ETE PSB-ECE/ETE	3	0	2		03	50	50	100	4
3	PCC	BEC503	Digital Communication	TD- ECE/ETE PSB-ECE/ETE	4	0	0		03	50	50	100	4
4	PCCL	BECL504	Digital Communication Lab	TD- ECE/ETE PSB-ECE/ETE	0	0	2		03	50	50	100	1
5	PEC	BEC515x	Professional Elective Course	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
6	PROJ	BEC586	Mini Project	TD- ECE/ETE PSB-ECE/ETE	0	0	4		03	100		100	2
7	AEC	BRMK557	**Research Methodology and IPR**		2	2	0		02	50	50	100	3
8	MC	BESK508	Environmental Studies	Any Department	2	0	0		02	50	50	100	2
9	MC	BNSK559	National Service Scheme (NSS)	NSS coordinator	0	0	2			100		100	0
		BPEK559	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK559	Yoga	Yoga Teacher									
									Total	**550**	**350**	**900**	**22**

Professional Elective Course

BEC515A	**Intelligent Systems and Machine Learning Algorithms**	BEC515C	Data Structure using C++
BEC515B	Digital Switching and Finite Automata Theory	BEC515D	Satellite and Optical Communication

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SXX**:

Semester End Evaluation. **K :** The letter in the course code indicates common to al the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

Mini-project work: Mini Project is a laboratory-oriented/hands on course that will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications etc. Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batches mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

No SEE component for Mini-Project.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering a professional elective is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

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Scheme of Teaching and Examinations2022

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2023-24)

VI SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BEC601	Embedded System Design	TD- ECE/ETE PSB-ECE/ETE	3	0	2		03	50	50	100	4
2	PCC	BEC602	VLSI Design and Testing	TD- ECE/ETE PSB-ECE/ETE	4	0	0		03	50	50	100	4
3	PEC	BEC613x	Professional Elective Course	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
4	OEC	BEC654x	Open Elective Course	TD- ECE/ETE PSB-ECE/ETE	3	0	0		03	50	50	100	3
5	PROJ	BEC685	Major Project Phase I	TD- ECE/ETE PSB-ECE/ETE	0	0	4		03	100	--	100	2
6	PCCL	BECL606	VLSI Design and Testing Lab	TD- ECE/ETE PSB-ECE/ETE	0	0	2		03	50	50	100	1
7	AEC/SDC	BEC657x	Ability Enhancement Course/Skill Development Course V	TD- ECE/ETE PSB-ECE/ETE	If the course is offered as a Theory 1	0	0		01	50	50	100	1
					If course is offered as a practical 0	0	2						
8	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
9	IKS	BIKS609	Indian Knowledge System		1	0	0		01	100	---	100	0
									Total	**600**	**300**	**900**	**18**

Professional Elective Course

BEC613A	**Multimedia Communication**	BEC613C	Digital Image Processing

BEC613B	Computer and Data Security	BEC613D	FPGA System Design using Verilog
Open Elective Course			
BEC654A	Digital System Design using Verilog	BEC654C	Electronic Communication Systems
BEC654B	Consumer Electronics	BEC654D	Basic VLSI Design
Ability Enhancement Course / Skill Enhancement Course-V			
BEC657A	FPGA System Design using Verilog LAB	BEC657C	IOT Lab
BEC657B	System Modelling using Simulink	BEC657D	Python Programming for Machine Learning Applications

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **K :** The letter in the course code indicates common to al the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course. **PROJ**: Project Phase -I, **OEC**: Open Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course ismandatory for the award of degree.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum number of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

Project Phase-I : Students have to discuss with the mentor /guide and with their helphe/she has to complete the literature survey and prepare the report and finally define the problem statement for the project work.

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VII SEMESTER (Swappable VII and VIII SEMESTER)

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BEC701	Microwave Engineering and Antenna Theory		3	0	2		03	50	50	100	4
2	IPCC	BEC702	Computer Networks and Protocols		3	0	2		03	50	50	100	4
3	PCC	BEC703	Wireless Communication Systems		4	0	0		03	50	50	100	4
4	PEC	BEC714x	**Professional Elective Course**		3	0	0		03	50	50	100	3
5	OEC	BEC755x	**Open Elective Course**		3	0	0		01	50	50	100	3
6	PROJ	BEC786	**Major Project Phase-II**		0	0	12		03	100	100	200	6
										350	**350**	**700**	**24**

Professional Elective Course

BEC714A	Application Specific Integrated Circuit	BEC714C	Automative Electronics
BEC714B	Cyber Security	BEC714D	Radar Communication

Open Elective Course

BEC755A	E-waste Management	BEC755C	Embedded System Applications
BEC755B	Automative Electronics	BEC755D	Sensors and Actuators

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **PEC**: Professional Elective Course, **OEC**: Open Elective Course PR: Project Work, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **TD-** Teaching Department, **PSB**: Paper Setting department, **OEC**: Open Elective Course, **PEC**: Professional Elective Course. **PROJ**: Project work

Note: VII and VIII semesters of IV years of the program

(1) Institutions can swap the VII and VIII Semester Schemes of Teaching and Examinations to accommodate research internships/ industry internships after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether the VII or VIII semesters is completed during the beginning of the IV year or the later part of IV years of the program.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum numbers of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

PROJECT WORK (21XXP75): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.

(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.

(iii) To impart flexibility and adaptability.

(iv) To inspire team working.

(v) To expand intellectual capacity, credibility, judgment and intuition.

(vi) To adhere to punctuality, setting and meeting deadlines.

(vii) To install responsibilities to oneself and others.

(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of the project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

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VIII SEMESTER (Swappable VII and VIII SEMESTER)

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PEC	BEC801x	**Professional Elective (Online Courses)**		3	0	0		03	50	50	100	3
2	OEC	BEC802x	**Open Elective (Online Courses)**		3	0	0		01	50	50	100	3
3	INT	BEC803	**Internship (Industry/Research) (14 - 20 weeks)**		0	0	12		03	100	100	200	10
										200	**200**	**400**	**16**

Professional Elective Course (Online courses)

BEC801A	BOS Recommended Course	BEC801C	BOS Recommended Course
BEC801B	BOS Recommended Course	BEC801D	BOS Recommended Course

Open Elective Courses (Online Courses)

BEC802A	BOS Recommended Course	BEC802C	BOS Recommended Course
BEC802B	BOS Recommended Course	BEC802D	BOS Recommended Course

L: Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **TD-** Teaching Department, **PSB**: Paper Setting department, **OEC**: Open Elective Course, **PEC**: Professional Elective Course. **PROJ**: Project work, **INT**: Industry Internship / Research Internship / Rural Internship

Note: VII and VIII semesters of IV years of the program

Swapping Facility

- Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate **research internships/ industry internships/Rural Internship** after the VI semester**.**
- Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.

Elucidation:

At the beginning of IV years of the program i.e., after VI semester, VII semester classwork and VIII semester **Research Internship /Industrial Internship / Rural Internship** shall be permitted to be operated simultaneously by the University so that students have ample opportunity for an internship. In other words, a good percentage of the class shall attend VII semester classwork and a similar percentage of others shall attend to Research Internship or Industrial Internship or Rural Internship.

Research/Industrial /Rural Internship shall be carried out at an Industry, NGO, MSME, Innovation center, Incubation centre, Start-up, centre of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations/institutes.

The mandatory Research internship /Industry internship / Rural Internshipis for 14 to 20 weeks. The internship shall be considered as a head of passing and shall be considered for the award of a degree. Those, who do not take up/complete the internship shall be declared to fail and shall have to complete it during the subsequent University examination after satisfying the internship requirements.

Research internship: A research internship is intended to offer the flavor of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.

Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.

Rural Internship: Rural development internship is an initiative of Unnat Bharat Abhiyan Cell, RGIT in association with AICTE to involve students of all departments studying in different academic years for exploring various opportunities in techno-social fields, to connect and work with Rural India for their upliftment.

The faculty coordinator or mentor has to monitor the student's internship progress and interact with them to guide for the successful completion of the internship.

The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of the internship.

With the consent of the internal guide and Principal of the Institution, students shall be allowed to carry out the internship at their hometown (**within or outside the state or abroad**), provided favorable facilities are available for the internship and the student remains regularly in contact with the internal guide. **University shall not bear any cost involved in carrying out the internship by students.** However, students can receive any financial assistance extended by the organization.

Professional Elective /Open Elective Course: These are ONLINE courses suggested by the respective Board of Studies. Details of these courses shall be made available for students on the VTU web portal.

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VI SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BXX601	Embedded System Design		3	0	2		03	50	50	100	4
2	PCC	BXX602	Microwave and Antenna Theory		4	0	0		03	50	50	100	4
3	PEC	BXX613x	Professional Elective Course		3	0	0		03	50	50	100	3
4	OEC	BXX654x	Open Elective Course		3	0	0		03	50	50	100	3
5	PCCL	BXXL606	Lab component		0	0	2		03	50	50	100	1
6	AEC/SDC	BXX657x	Ability Enhancement Course/Skill Development Course V		If the course is offered as a Theory: 1	0	0		01	50	50	100	1
					If course is offered as a practical: 0	0	2						
7	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
8	IKS	BIKS609	Indian Knowledge System		1	0	0		01	100	---	100	0
									Total	**500**	**300**	**800**	**16**

Professional Elective Course			
BEC613A	Intelligent Systems and Machine Learning Algorithms	BEC613C	Digital Image Processing
BEC613B	Computer and Data Security	BEC613D	FPGA System Design using Verilog
Open Elective Course			
BEC654A	Digital System Design using Verilog	BEC654C	Electronic Communication Systems

BEC654B	Consumer Electronics	BEC654D	Basic VLSI Design
Ability Enhancement Course / Skill Enhancement Course-V			
BEC657A	FPGA System Design using Verilog LAB	BEC657C	IOT Lab
BEC657B	System Modelling using Simulink	BEC657D	Python Programming for Machine Learning Applications

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VII and VIII semester for who seeks internship with project work

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PCC	BXX701	To be completed in 5th / 6th semester		3	0	2		03	50	50	100	4
2	PCC	BXX702	To be completed in 5th / 6th semester		3	0	2		03	50	50	100	4
3	PCC	BXX703	To be completed in 5th / 6th semester		4	0	0		03	50	50	100	3
4	PEC	BXX714x	Professional Elective Course (MOOC Courses)		3	0	0		03	50	50	100	3
5	OEC	BXX755x	Open Elective Courses(MOOC courses)		3	0	0		01	50	50	100	3
1	PEC	Bxx801x	Professional Elective (Online Courses)		3	0	0		03	50	50	100	3
2	OEC	Bxx802x	Open Elective (Online Courses)		3	0	0		01	50	50	100	3
3	PROJ	BXX883	Project Work Outcome of Training		0	0	12		03	100	100	200	9
4	INT	Bxx804	Internship (Industry/Research) (Two semesters)		0	0	12		03	100	100	200	10
									Total	**200**	**200**	**400**	**42**

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – V

Technological Innovation and Management Entrepreneurship

Course Code	BEC501	**CIE Marks**	**50**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**50**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS-03

Course Learning Objectives: This course will enable students to:

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills.
- Identify the Management functions and Social responsibilities.
- Understand economic development, creativity and Innovation.
- Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding.

MODULE-1	RBT Level
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession **(Selected topics of Chapter 1, Text1).** **Planning:** Planning**-**Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making (**Selected topics from Chapters 4 & 5, Text 1).**	**L1,L2**
MODULE-2	
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance**,** Recruitment and Selection Process **(Selected topics from Chapters 7, 8 & 11,Text 1).** **Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (**Selected topics from Chapters 15 to 18 and 9, Text 1).**	**L1,L2**
MODULE-3	
Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance **(Selected topics from Chapter 3, Text 1).** **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **(Selected topics from Chapter 2, Text 2).**	**L1,L2**
MODULE-4	

Modern Small Business Enterprises: Role of Small Scale Industries, Impact of Globalization and WTO on SSIs, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Ancillary Industry and Tiny Industry (Definition only) (**Selected topics from Chapter1, Text 2**). **Idea Generation and Feasibility Analysis-** Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.**(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)**	**L1,L2**
MODULE-5	
Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? **(Selected topics from Chapter 8 (Page No 159-164, Text 2)** **Financing and How to start a Business?** Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise **(Selected topics from Chapter 7(Page No 147-149), Chapter 5 (Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)** **Project Design and Network Analysis:** Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences**.(Selected topics from Chapters 20, Text 3).**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
2. Describe the functions of Managers, Entrepreneurs and their social responsibilities
3. Understand the components in developing a business plan, along with the integration of CSR-Corporate Social Responsibility.
4. Describe the importance of small scale industries in economic development and institutional support to start a small scale industry and understand the concepts of Creativity and Innovation and Identification of Business Opportunities.
5. Awareness about various sources of funding and institutions supporting entrepreneurs

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-graw Hill Publishing Co.ltd.-new Delhi, 2012.

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

Digital Signal Processing		Semester	5
Course Code	**BEC502**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1. Preparation: To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
2. Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms, their properties, efficient computations & the design of digital filters.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teachingmethods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes criticalthinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinkingskills such as the ability to evaluate, generalize, and analyze information rather than simply recallit.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up withtheir own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helpsimprove the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and havediscussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1

Introduction: Signals, Systems and Signal Processing, Classification of Signals, The Concept of Frequency in Continuous Time and Discrete Time Sinusoidal Signals. [Text1: 1.1, 1.2, 1.3: 1.3.1, 1.3.2]

Discrete Time Signals and Systems: Discrete Time Signals, Discrete Time Systems, Analysis of Discrete Time Linear Time Invariant Systems.

[Text 1: 2.1.1, 2.1.2, 2.2.1, 2.2.2, 2.2.3, 2.3.1, 2.3.2, 2.3.3, 2.3.5]

MODULE-2

Z-Transforms: The z-Transform, Properties of the z-Transform (Statements only), The System Function of a Linear Time Invariant system. Text1:3.1, 3.2, 3.3.3.

The Discrete Fourier Transform: Frequency Domain sampling and Reconstruction of Discrete Time Signals, The DFT, The DFT as Linear Transformation. Properties of DFT: Periodicity, Linearity and Symmetry for real valued sequence, Multiplication of two DFTs and Circular Convolution.

[Text1: 7.1.1, 7.1.2, 7.1.3, 7.2: 7.2.1, 7.2.2]

MODULE-3

DFT Properties: Time reversal of a sequence, Circular Time shift of a sequence, Circular frequency shift, Complex conjugate property, Multiplication of two sequences, Perceval's theorem. Linear Filtering Methods based on the DFT. (Text 1: 7.3].

Efficient Computation of the DFT- FFT Algorithms: Direct Computation of the DFT, Radix-2 FFT Algorithms: computation of DFT and IDFT in decimation in time.

[Text1: 8.1: 8.1.1, 8.1.3].

MODULE-4

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Bartlett, Hanning, Hamming and Blackman windows. Structure for FIR Systems: Direct form and Cascade form. [Text1: 10.1.2, 10.2.1, 10.2.2]
MODULE-5
IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design (Lowpass and Highpass) using BLT. Realization of IIR Filters in Direct form I and II. [Text2: 8.1, 8.2, 8.3 (Butterworth filter design), 8.8.1]

PRACTICAL COMPONENT OF IPCC

List of Programs to be implemented & executed using any programming languages like **Moku:Go/ MATLAB/OCTAVE (but not limited to)**

Sl.NO	Experiments
1	Program to generate the following discrete time signals. a) Unit sample sequence, b)Unit step sequence, c) Exponential sequence, d)Sinusoidal sequence, e) Random sequence
2	Program to perform the following operations on signals. a) Signal addition, b) Signal multiplication, c)Scaling, d) Shifting, e)Folding
3	Program to perform convolution of two given sequences (without using built-in function) and display the signals.
4	Consider a causal system y(n) = 0.9y(n-1)+x(n). a) Determine H(z) and sketch its pole zero plot. b) Plot $\|H(e^{j\omega})\|$ and $\angle H(e^{j\omega})$ c) Determine the impulse response h(n).
5	Computation of N point DFT of a given sequence (without using built-in function) and to plot the magnitude and phase spectrum.
6	Using the DFT and IDFT, compute the following for any two given sequences a)Circular convolution b) Linear convolution
7	Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
8	Develop decimation in time radix-2 FFT algorithm without using built-in functions.
9	Design and implementation of digital low pass FIR filter using a window to meet the given specifications
10	Design and implementation of digital high pass FIR filter using a window to meet the given specifications
11	Design and implementation of digital IIR Butterworth low pass filter to meet the given specifications.
12	Design and implementation of digital IIR Butterworth high pass filter to meet the given specifications

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Analyse the different types of signals and systems used in digital signal processing.
- Compute the response of an LTI system using time and frequency domain techniques.
- Develop algorithms for the efficient computations of DFT and IDFT.
- Design of digital FIR filters for the given specifications using different window methods.
- Design of digital IIR digital filters using bilinear transformation method.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100)

in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Text Books:

1. Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.
3. Vinay K. Ingle, John G Proakis , "Digital Signal Processing Using MATLAB, A problem Solving Companion", Cengage Learning, 2018, ISBN: 93-86668-11-4

Reference Books:

1. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.
2. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2017. ISBN:978-1-25-909858
3. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003.
4. D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web links and Video Lectures (e-Resources):

1. Digital Signal processing, https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

DIGITAL COMMUNICATION		Semester	5
Course Code	**BEC503**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Understand the principles of spread spectrum communications.
- Understand the basic principles of information theory and various source coding techniques.
- Build a comprehensive knowledge about various Source and Channel Coding techniques.
- Discuss the different types of errors and error detection and controlling codes used in the communication channel.
- Understand the concepts of convolution codes and analyze the code words using time domain and transform domain approach.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Arrange visits to nearby PSUs such as BHEL, BEL, ISRO, etc., and small-scale communication industries.
3. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
4. Encourage collaborative (Group) Learning in the class
5. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
9. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Bandpass Signals to Equivalent Lowpass: Hilbert Transform, Pre-envelopes, Complex envelopes of Band-pass Signals, Canonical Representation of Bandpass signals.

Signalling over AWGN Channels- Introduction, Geometric representation of signals, Gram- Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel , Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.

Module-2

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. BFSK using Noncoherent Detection, Differential Phase Shift Keying.

Module-3

Information theory: Introduction, Entropy, Source Coding Theorem, Lossless Data Compression Algorithms, Discrete Memoryless Channels, Mutual Information, Channel capacity, Channel Coding Theorem, Information Capacity Law (Statement).

Module-4

Error Control Coding: Error Control Using Forward error Correction,
Linear Block Codes: Definitions, Matrix Descriptions, Syndrome and its properties, Minimum distance Considerations, Syndrome Decoding, Hamming Codes.
Cyclic Codes: Properties, Generator and Parity Check Polynomial and matrices, Encoding, Syndrome computation, Examples.

Module-5

Convolutional Codes: Convolutional Encoder, Code tree, Trellis Graph and State graph, Recursive systematic Convolutional codes, Optimum decoding of Convolutional codes, Maximum Likelihood Decoding of Convolutional codes: The Viterbi Algorithm, Examples.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Apply the concept of signal conversion to vectors in communication transmission and receiption.
2. Perform the mathematical analysis of digital communication systems for different modulation techniques.
3. Apply the Source coding and Channel coding principles for the discrete memoryless channels.
4. Compute the codewords for the error correction and detection of a digital data using Linear Block Code, Cyclic Codes and Convolution Codes.
5. Design encoding and decoding circuits for Linear Block Code, Cyclic Codes and Convolution Codes.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81- 265-4231-4.

Reference Books

1. B.P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems",4th Edition, Oxford University press, ISBN: 9780198073802, 2017
2. K Sam Shanmugam, "Digital and analog communication systems", Wiley India Pvt. Ltd, 2017, ISBN:978-81-265-3680-1,.
3. K.N Hari Bhat, D. Ganesh Rao, "Information Theory and Coding", Cengage Learning India Pvt Ltd, 2017, ISBN: 93-866-5092-4,.

Web links and Video Lectures (e-Resources):
1. Principles of Communication Systems Part II, https://onlinecourses.nptel.ac.in/noc19_ee47/preview
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning 1. Experiential Learning by using free and open source software's SCILAB or OCTAVE or Python

Intelligent Systems and Machine Learning Algorithms		Semester	5
Course Code	**BEC515A**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Gain a historical perspective of AI and its foundations.
- Become familiar with basic principles of AI toward Problem-Solving
- Get to know approaches of inference, perception, knowledge representation, and learning
- Define Machine Learning and understand the basic theory underlying machine learning.
- Differentiate supervised, unsupervised, and reinforcement learning

Teaching-Learning Process (General Instructions)

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These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method; different teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as evaluating, generalizing, and analyzing information rather than simply recalling it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction: What is AI? Foundations and History of AI Intelligent Agents: Agents and environment, Concept of Rationality, The nature of environment, The structure of agents.

Text book 1: Chapter 1- 1.1, 1.2, 1.3 Chapter 2- 2.1, 2.2, 2.3, 2.4

Module-2

Problem-solving: Problem-solving agents, Example problems, Searching for Solutions Uninformed Search Strategies: Breadth First search, Depth First Search, Iterative deepening depth first search;

Text book 1: Chapter 3- 3.1, 3.2, 3.3, 3.4

Module-3

Informed Search Strategies: Heuristic functions, Greedy best first search, A*search. Heuristic Functions Logical Agents: Knowledge–based agents, The Wumpus world, Logic, Propositional logic, Reasoning patterns in Propositional Logic

Text book 1: Chapter 3-3.5,3.6 Chapter 4 – 4.1, 4.2 Chapter 7- 7.1, 7.2, 7.3, 7.4, 7.5

Module-4
Introduction: Machine learning Landscape: what is ML?, Why, Types of ML, main challenges of ML Concept learning and Learning Problems – Designing Learning systems, Perspectives and Issues – Concept Learning – Find S-Version Spaces and Candidate Elimination Algorithm – Remarks on VS- Inductive bias. Text book 3: Chapter 1, Textbook 4:Chapter 1 and 2
Module-5
End-to-end Machine learning Project: Working with real data, Look at the big picture, Get the data, Discover and visualize the data, Prepare the data, select and train the model, Fine tune your model. Classification: MNIST, training a Binary classifier, performance measure, multiclass classification, error analysis, multi-label classification, multi-output classification Textbook 4: Chapter 2, Chapter 3
Course outcome (Course Skill Set) At the end of the course, the student will be able to: CO1. Apply knowledge of agent architecture, searching, and reasoning techniques for different Applications. CO 2. Compare various Searching and Inferencing Techniques. CO 3. Develop knowledge base sentences using propositional logic and first-order logic CO 4. Understand the concept of Machine Learning and Concept Learning. CO 5. Apply the concept of ML and various classification methods in a project

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015
2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.
3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013
4. Aurelien Geron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.

Reference Books:

1. George F Lugar, Artificial Intelligence Structure and strategies for complex, Pearson Education, 5th Edition, 2011
2. Nils J. Nilsson, Principles of Artificial Intelligence, Elsevier, 1980
3. Saroj Kaushik, Artificial Intelligence, Cengage learning, 2014.

4. Ethem Alpaydin, Introduction to Machine Learning, PHI Learning Pvt. Ltd, 2nd Ed., 2013
5. T. Hastie, R. Tibshirani, J. H. Friedman, The Elements of Statistical Learning, Springer, 1st edition, 2001
6. Machine Learning using Python, Manaranjan Pradhan, U Dinesh Kumar, Wiley, 2019
7. Machine Learning, Saikat Dutt, Subramanian Chandramouli, Amit Kumar Das, Pearson,2020

Web links and Video Lectures (e-Resources):

- NPTEL Video lectures: https://nptel.ac.in/courses/106105077
- NPTEL Video lectures: https://nptel.ac.in/courses/106102220
- https://archive.nptel.ac.in/courses/106/105/106105152
- https://archive.nptel.ac.in/courses/106/106/106106202
- https://nptel.ac.in/domains/discipline/106?course=106_0

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Mini projects.

Digital Switching and Finite Automata Theory			
Course Code	**BEC515B**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	42	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

1. To understand the basics of switching theory, including combinational logic design and testing.
2. To learn finite-state machine design and testing, essential for modeling computational processes.
3. To illustrate methods for logic synthesis and optimization, crucial for efficient digital system design.
4. To understand the modern topics such as CMOS gates, logic design for emerging nanotechnologies, digital system testing, and asynchronous circuit design
5. To assess the practical examples to reinforce the learning and application concepts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Logic design: Design with basic logic gates, Logic design with integrated circuits, NAND and NOR circuits, Design of high-speed adders, Metal-oxide semiconductor (MOS) transistors and gates(5.1 to 5.6 of Text1) **Threshold Logic:** Introductory Concepts: Threshold element, capabilities and limitations of threshold logic, Elementary Properties, Synthesis of Threshold networks: Unate functions, Identification and realization of threshold functions, The map as a tool in synthesizing threshold networks. (Sections 7.1, 7.2 of Text 1)

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, **RBT Level:** L1, L2, L3

Module-2	
Testing for Combinational circuits Fault models, Structural testing, IDDQ testing, Delay fault testing, Synthesis for testability, Testing for nanotechnologies (8.1 to 8.6 of Text1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation, YouTube videos, **RBT Level:** L1, L2, L3
Module-3	
Finite-state machines: Introduction to synchronous sequential circuits and iterative networks, Sequential circuits – introductory example, The finite-state model – basic definitions, Memory elements and their excitation functions, Synthesis of synchronous sequential circuits, An example of a computing machine, Iterative networks (9.1 to 9.6 of Text1) **Capabilities, minimization, and transformation of sequential machines** The finite-state model – further definitions, Capabilities and limitations of finite-state machines State equivalence and machine minimization, Simplification of incompletely specified machines (10.1 to 10.4 Text1)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTubevideos **RBT Level:** L1, L2, L3
Module-4	
Asynchronous sequential circuits: Modes of operation, Hazards, Synthesis of SIC fundamental-mode circuits. **Structure of Sequential Machines:** Introductory example, State assignment using partitions: closed partitions, The lattice of closed partitions, Reduction of output dependency, Input dependence and autonomous clocks, Covers and generation of closed partitions by state splitting: Covers, The implication graph, An application of state splitting to parallel decomposition. (Section 11.1, 11.2, 11.3, 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 of Text1)	
Teaching-Learning Process	Chalkandtalkmethod, PowerPoint Presentation, YouTube videos, **RBT Level:** L1, L2, L3
Module-5	
Memory, definiteness, and information loss lessness of finite automata Memory span with respect to input–output sequences (finite-memory machines), Memory span with respect to input sequences (definite machines), Memory span with respect to output sequences, Information-lossless machines(14.1 to 14.4 of Text1)	
Teaching-Learning Process	Chalk and talk method/Power point presentation, YouTube videos **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Make use of mapping tool to synthesize threshold logic
2. Analyze effects of hazards and fault diagnosis in digital logical circuits
3. Examine the capabilities of Finite State Machines by minimization Procedures
4. Model the structures of sequential machines
5. Develop the methods of state identification and fault detection
6. Design the fault detection algorithm

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
    1. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. Switching and Finite Automata Theory – Zvi Kohavi and Niraj K. Jha, Cambridge University press, 3rd edition, 2010.

Reference Books:

2. Introduction to switching theory and logic design Fredriac J. Hill, Gerald Peterson, 3rd edition,
3. Fault Tolerant and Fault Testable Hardware Design-Parag K Lala, Prentice Hall Inc. 1985.
4. Digital Circuits and Logic Design. -Charles Roth Jr, Larry L. Kinney, Cengage Learning, 2014, ISBN: 978-1-133-62847-7.

Web links and Video Lectures (e-Resources)

https://onlinecourses.nptel.ac.in/noc20_cs67

https://onlinecourses.nptel.ac.in/noc24_cs61

Data Structures using C++		Semester	5
Course Code	**BEC515C**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- Learn the Basic Concepts of C++
- Describe the concepts of Pointers and Arrays
- Concepts of Data Structures
- Understanding of the implementation of a linked list and Algorithms

Teaching-Learning Process (General Instructions)

These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. **Online coding platforms can be used to execute programs**
2. **Mobile applications can be used to execute the codes.**
3. **Presentation of concepts**

Module-1

UNIT-I: Software Engineering Principles And C++ Classes

Software Life Cycle, Software Development Phase, Classes.
Page No. 1-7, 17-33
OOD: Inheritance, Polymorphism, Templates
Page No. 60-78,84-112

UNIT-II: Pointers & Array based Lists

Pointer Data Type and Pointer Variables, Classes & Pointers, Inheritance Pointers &Virtual functions, Abstract Classes & Pure Virtual functions, Array Based Lists
Page No. 131-183

Module-2

UNIT-III: Linked Lists &Stacks

Linked List, Linked List as an ADT, Unordered Linked List, ordered Linked List, Doubly Linked Lists
Page No. 265-320
Stack: Stacks, Implementation of Stacks as Arrays , Linked Implementation of Stacks
Page No. 395-428

Module-3

UNIT-IV: Queues and Algorithms

Queue Operations, Implementation of Queues as Arrays, Linked Implementation of Queues, STL class queue, Priority Queues, Application of Queues: Simulation.
Page No. 451-490
Search Algorithms, Hashing, Sorting Algorithms: Selection sort, Insertion sort, Shell Sort.
Page No. 497-524,533-550

Module-4

UNIT-V: Binary Trees and B-Trees

Binary Trees, Binary Tree Traversal, Binary Search Trees, Binary Search Tree: Analysis, Non-recursive Binary Tree Traversal Algorithms, Binary Tree Traversal and Functions as Parameters, AVL (Height-Balanced) Trees, B-Trees
Page No. 599-675

Module-5

UNIT-VI: Graphs

Introduction, Graph Definitions and Notations, Graph Representation, Operations on Graphs, Graphs as ADTs, Graph Traversals, Shortest Path Algorithm, Minimum Spanning Tree, Topological Order, Euler Circuits

Page No.685-721

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Distinguish between procedures and object-oriented programming.
2. Apply advanced data structure strategies for exploring complex data structures.
3. Compare and contrast various data structures and design techniques in Performance.
4. Implement data structure algorithms through C++. Incorporate data structures into the applications such as binary search trees, AVL, and B Trees
5. Implement all data structures like stacks, queues, trees, lists, and graphs and compare their Performance and trade-offs.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Text Book:

1.D.S.Malik - Data Structures using C++2nd Edition.

Reference Book

1. Sartaj Sahni – Data Structures, Algorithms, and Applications in C++ 2nd Edition

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/106106127
- https://nptel.ac.in/courses/106102064
- https://nptel.ac.in/courses/106106133

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Students Can use Mobile applications/Online compilers/Code blocks to execute the programs and check output for different cases.

Satellite and Optical Communication		Semester	V
Course Code	BEC515D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	03	Exam Hours	
Examination type (SEE)	Theory/practical/Viva-Voce /Term-work/Others		

Course objectives:

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the communication satellite.
- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses, optical components and its applications in optical communication.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. [Text 1: 2.1,2.2,2.3,2.4,2.5,3.3,3.4,3.5,3.6,3.7] L1, L2

Module-2

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.

Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.

[Text 1: 4.1,4.5,4.6,4.7,4.8, 8.1,8.2,8.3,8.4,8.5,8.6,8.7] L1, L2

Module-3

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.
[Text 1: 9.1,9.2,9.3,9.4,9.5,9.6,9.7,9.8,9.10] L1, L2

Module-4

Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials. Attenuation and Dispersion: Attenuation, Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion. [Text 2 : 2.3[2.3.1 to 2.3.4], 2.4[2.4.1, 2.4.2],2.5, 2.7],3.1, 3.2 L1, L2, L3

Module-5

Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes.

WDM Concepts: Overview of WDM, Isolators and Circulators, Fiber grating filters (No derivation), Dielectric thin-film filters, Diffraction Gratings.
[Text 2: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7] L1, L2

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
2. Describe the Electronic hardware systems associated with the satellite subsystem and earth station.
3. Describe the communication satellite with the focus on national satellite system.
4. Classification and characterization of optical fibers with different modes of signal propagation.
5. Describe the constructional features and the characteristics of optical fiber and optical devices used for signal transmission and reception.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Book:

1. Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.
2. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4
3. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
4. Theodore Rappaport, Wireless Communications: Principles and Practice, 2nd Edition,

Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/courses/117105131 • Basic Introduction To Satellite Communications | Satellite Communications - YouTube • How Satellite Works (Animation) - YouTube • Introduction video: Fiber Optic Communication Technology (youtube.com) • Introduction (youtube.com) (Introduction to Fiber optics)

Digital Communication Lab		Semester	5
Course Code	**BECL504**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination type (SEE)	**Practical**		

Course objectives:

This laboratory course enables students to

- Design of basic digital modulation techniques using electronic hardware.
- Simulation of vector computations and derive the orthonormal basis set using Gram Schmidt procedure.
- Simulate the digital transmission and reception in AWGN channel
- Simulate the digital modulations using software and display the signals and its vector representations.
- Implement the source coding algorithms using a suitable software platform.
- Simulate the channel coding techniques and perform decoding for error detection and correction.

Sl.NO	Experiments
	Hardware Experiments
1	Generation and demodulation of the Amplitude Shift Keying signal.
2	Generation and demodulation of the Phase Shift Keying signal.
3	Generation and demodulation of the Frequency Shift Keying signal.
4	Generation of DPSK signal and detection of data using DPSK transmitter and receiver.
Simulation Experiments (Use MUKU:GO / MATLAB / Scilab /LabVIEW or any other suitable software)	
5	Gram-Schmidt Orthogonalization: To find orthogonal basis vectors for the given set of vectors and plot the orthonormal vectors.
6	Simulation of binary baseband signals using a rectangular pulse and estimate the BER for AWGN channel using matched filter receiver.
7	Perform the QPSK Modulation and demodulation. Display the signal and its constellation.
8	Generate 16-QAM Modulation and obtain the QAM constellation.
9	Encoding and Decoding of Huffman code.
10	Encoding and Decoding of binary data using a Hamming code.
11	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify for the cases, a) Without error b) With error
12	Encoding and Decoding of Convolution code

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design the basic digital modulation and demodulation circuits for different engineering applications.
2. Design of optimum communication receivers for AWGN channels.
3. Illustration of different digital modulations using the signals and its equivalent vector representations.
4. Implement the source coding and channel coding procedures using suitable software.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall

be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.
The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. B. P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems" 4th Edition, Oxford University Press, 2017, ISBJ:978-0-19-947628-2
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication Systems", Mc Graw Hill Education, 2013, ISBN: 978-1-25-902985-1.

	Embedded System Design	Semester	06
Course Code	BEC601	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory		

Course objectives:

- Identify various components, their purpose, and their application to the embedded system's applicability.
- Program various embedded components using the embedded C program.
- Understand the embedded system's real-time operating system and its application in IoT
- Understand the fundamentals of ARM-based systems, including architecture and its units like registers , debug interface, stack, MPU, Interrupts etc
- Use the various instructions to program the ARM controller.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

MODULE-1

Introduction to Embedded System: What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Major Application Areas of Embedded Systems. Purpose of Embedded Systems, The Typical Embedded System, Microprocessor Vs Microcontroller, Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors, Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7-Segment LED Display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface, External Communication Interface, Embedded Firmware, Other System Components

(Text 1: All the Topics from Ch-1 and Ch-2.)

MODULE-2

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).

Text 1: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)
MODULE-3
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil). **(Text 1: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2 only), Ch-12, Ch-13 (a block diagram before 13.1, only).**
MODULE-4
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2: Chapter 1, 2**
MODULE-5
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2: Chapter 3**

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn Assembly Language Program and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

Sl.NO	Experiments
1	Write a program to find the sum of the first 10 integer numbers.
2	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3	Write a program to find the factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5	Write a program to find the square of a number (1 to 10) using a look-up table.
6	Write a program to find the largest or smallest number in an array of 32 numbers.
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	Write a program to count the number of ones and zeros in two consecutive memory locations.
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Understand the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. **Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education**
2. **Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.**

Reference Book

1. **Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.**

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105193/
2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference
3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/
4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors
5. https://alison.com/tag/embedded-systems

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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	VLSI Design and Testing	Semester	5
Course Code	**BEC602**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1.This course deals with analysis and design of digital CMOS integrated circuits.

2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.

3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.

4. Understanding the CMOS sequential circuits and memory design concepts.

5.Explore the knowledge of VLSI Design flow and Testing

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.

[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

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Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3.

MODULE-3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.
[Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:
Chalk and talk method/Power point presentation, YouTube Videos RBT Level: L1, L2, L3.

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.

[Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:
Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.
[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction**,** Design Styles, Testing
[Text1: 6.1, 6.2. 6.5]

Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Course Outcomes: After completing the course, the students will be able to

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CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
C05	Understand the concepts of Sequential circuits design and VLSI testing

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	Multimedia Communication		Semester	6
	Course Code	**BCE613A**	CIE Marks	50
	Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	
	Examination type (SEE)	Theory		

Course objectives:

- Gain fundamental knowledge in understanding the basics of different multimedia Networks and applications.
- Understand digitization principle techniques required to analyze different media Types.
- Analyze compression techniques required to compress text and image and gain Knowledge of DMS.
- Analyze compression techniques required to compress audio and video.
- Gain fundamental knowledge about multimedia communication across different Networks.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text1)

Module-2

Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1

Module-3

Text and Image Compression: Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1)

Module-4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)

Module-5

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI (Chapter 8.1 to8.6of Text 1).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the basics of multimedia Communication and applications
2. Analyze media types to represent them in digital form.
3. Apply the compression techniques on text, images, audio and video.
4. Understand multimedia information networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks:

Multimedia Communications –Fred Halsall, Pearson Education,2001,ISBN-978813170994

ReferenceBooks:

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. FundamentalsofMultimedia–Ze-NianLi,MarkSDrew,andJiangchuanLiu.

Web links and Video Lectures (e-Resources):

- Implementation of compression algorithms using MATLAB/any open source tools (Python, Scilab, etc.)

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- https://www.slideshare.net
  NPTEL Video Lectures
- https://archive.nptel.ac.in/courses/117/105/117105083/
- Multimedia Computing lecture: Communications & Networking –You Tube

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

Data Security

Course Code	**BEC613B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
CREDITS - 03			

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, authentication functions like HASH codes, MACs, digital signatures, as well as key distribution

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1	RBTL Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques (excluding Hill cipher) (Text 1: Chapter 1: Section 1, 2) **Block Ciphers**: Traditional Block Cipher structure, (Text 1: Chapter 2: Section1) The AES Cipher. (Text 1: Chapter 4: Section 2,4) Block Cipher Modes of Operation (Text 1: Chapter 5: Section 2, 3, 4, 5, 6)	L1, L2, L3
MODULE-2	
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Fields of the Form GF(2_m) (Text 1: Chapter 3)	L1, L2, L3
MODULE-3	

More on Number Theory: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5) **ASYMMETRIC CIPHERS**: Principles of Public-Key Cryptosystems, The RSA algorithm (Text 1: Chapter 8: Section 1, 2), Diffie – Hellman Key Exchange, Elliptic Curve Arithmetic over Z_p, Elliptic Curve Cryptography (Text 1: Chapter 9: Section 1, 3, 4)	L1, L2, L3
MODULE-4	
Cryptographic Hash Functions: Application of Hash Functions, Two Simple Hash Functions, Requirements and Security, Hash function based on Cipher Block Chaining, SHA-512 (Only structural description). (Text 1: Chapter 10: Section 1, 2, 3, 4, 5) **Message Authentication Codes:** Message Authentication Functions, Security of MACs, MACs based on Hash Functions. (Text 1: Chapter 11: Section 2, 4, 5)	L1, L2, L3
MODULE-5	
Digital Signatures: Digital Signatures, NIST Digital Signature Algorithm, Elliptic Curve Digital Signature Algorithm. (Text 1: Chapter 12: Section 1, 4, 5) **Key Management and Distribution:** Symmetric Key Distribution Using Symmetric Encryption, Symmetric Key Distribution Using Asymmetric Encryption, Distribution of Public Keys (Text 1: Chapter 13: Section 1, 2, 3)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain traditional cryptographic algorithms of encryption and decryption process.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
- Apply concepts of modern algebra in cryptography algorithms.
- Explain message authentication using HASH functions, MAC functions and Digital signatures.
- Explain how symmetric and asymmetric encryption algorithms can be used to distribute keys.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

Reference Books

1. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
2. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/105/106105162

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VI Semester

Digital Image Processing			
Course Code	**BEC613C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

<table>
<tr><th colspan="2">Module-2</th></tr>
<tr><td colspan="2">Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform.
Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications.
Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform.
Practical topics: Problems on DFT and DCT
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-3</th></tr>
<tr><td colspan="2">Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
[Text: Chapter 3: Sections 3.2 to 3.6]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters.
Self-study topics: Point, line and edge detection.
Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-4</th></tr>
<tr><td colspan="2">Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.
Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.
[Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing.
Self-study topics: Basic concept of segmentation.
Practical topics: Problems on Pseudo-color Image Processing
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-5</th></tr>
<tr><td colspan="2">Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and their applications.
Self-study topics: Linear position invariant degradation, Estimation of degradation function.
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="2">Course outcomes (Course Skill Set)
At the end of the course the student will be able to:
1. Understand image formation and the role of human visual system plays in the perception of gray andcolor image data.
2. Compute various transforms on digital images.
3. Conduct an independent study and analysis of Image Enhancement techniques.
4. Apply image processing techniques in the frequency (Fourier) domain.
5. Design image restoration techniques.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based Learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

FPGA Based System design Using Verilog		Semester	VI
Course Code	BEC613D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

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1. Lecture method (L) does not mean only traditional lecture method, but different types of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction to Programmable Logic Devices:

Hazards in Combinational Circuits, Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs)
Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)

(Text 1: 1.5,3.1,3.2 , 3.3, 3.4) RBT Level: L1, L2, L3

Module-2

Advanced Digital Design Examples:
BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light controller, Synchronization and debouncing, Shift-and-Add Multiplier
Array Multiplier, A Signed Integer/Fraction Multiplier, (Excluding Test Bench) , Keypad Scanner (Excluding Test Bench)

Module-3

SM Charts and Microprogramming :
State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier , Dice Game (Excluding Test Bench) , Realization of SM Charts , Implementation of the Dice Game . Microprogramming , Linked State Machines.
(**Text 1: 5.1, 5.2, 5.3 , 5.4 , 5.5 , 5.6) RBT Level:** L1, L2, L3

Module-4

Floating-Point Arithmetic: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations.
Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Rise and Fall Delays of Gates

(Text 1:7.1,7.2, 7.3,7.4, 8.3, 8.4, 8.5,8.6,8.8) RBT Level: L1, L2, L3

Module-5

Designing with Field Programmable Gate Arrays :
Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition Carry Chains in FPGAs , Cascade Chains in FPGAs , Examples of Logic Blocks in Commercial FPGAs , Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates , Design Translation.

(Text 1: 6.1,6.2,6.3, 6.4 ,6.5 , 6.6, 6.7, 6.8,6.10, 6.11) RBT Level: L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Apply the concept of Programmable logic devices to implement digital design.
2. Design and implementation of Advanced logic design using Verilog HDL
3. Understand the concept of SM Chart and design complex digital circuits using SM Chart.
4. Performing the Floating-point arithmetic operations and designing of Memories
5. Designing and performance evaluation of advanced digital design using FPGAs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1 Digital Systems Design Using Verilog First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John The University of Texas at Austin, Byeong Kil Lee The University of Texas at San Antonio

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum

2. ASIC and FPGA Verification: A guide to component Modelling.
Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier

3. Processor Design . System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland Tampere University of Technology Sringer Publications.

4. The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

Activity Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's

Digital System Design using Verilog		Semester	6
Course Code	**BEC654A**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Functions.
- Understand Timing and Delay Simulation.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

Overview of Digital Design with Verilog HDL: Evolution of Computer-Aided Digital Design (CAD), Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. (**Text 1: 1.1 to 1.6**)

Hierarchical Modeling Concepts: Design Methodologies, Top-down and Bottom-up design methodology, Modules, Instances, Components of a Simulation, Design Block, Stimulus Block (Test Bench) with example. **(Text 1:2.1 to 2.6)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Basic Concepts: Lexical Conventions, Data Types, System Tasks, Compiler Directives. **(Text 1: 3.1 to 3.3)**

Modules and Ports: Modules, Ports, Connecting Ports, Hierarchical Names. **(Text 1: 4.1 to 4.3)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Gate-Level Modeling: Gate Types-Modeling using basic Verilog gate primitives, Description of AND/OR and BUF/NOT type gates. Gate Delays-Rise, Fall and Turn-Off Delays, Min, Max and Typical Delays. **(Text1: 5.1, 5.2)** **Dataflow Modeling**: Continuous assignments, Delay Specification, Expressions, Operators, Operands, Operator Types, Examples **(Text 1: 6.1 to 6.5)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Behavioral Description: Structured Procedures, Initial and Always statements, Procedural Assignments Blocking and Non-Blocking statements, Conditional statements, Multiway Branching, Loops, Sequential and Parallel blocks, Examples-4-to-1 Multiplexer, 4-bit Counter. **(Text 1: 7.1, 7.2, 7.4, 7.5, 7.6, 7.7, 7.9.1, 7.9.2)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Structural Description: Highlights of Structural Descriptions, Organization of Structural Description, Binding **(Text 2: 4.1, 4.2, 4.3, Listings 4.1 to 4.13 only Verilog)** **Tasks and Functions**: Differences between Tasks and Functions, Declaration and Invocation, Examples **(Text 1: 8.1, 8.2, 8.2.1, 8.2.2, 8.3, 8.3.1, 8.3.2)**	

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the Verilog HDL design flow.
2. Describe the basic concepts of Verilog HDL programming.
3. Write Verilog programs in Gate, Dataflow, Behavioral, and structural modeling levels of Abstraction.
4. Write the programs more effectively using Verilog Tasks and Functions.
5. Perform Timing and Delay Simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier

	Consumer Electronics		Semester	6
	Course Code	**BEC654B**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- To understand the working principles and classifications of various microphones and loudspeakers, and their roles in audio systems.
- To explore the structure, recording, and playback processes of Audio Compact Disc systems, along with error correction techniques and digital-to-analog conversion.
- To analyse the fundamentals of colour television systems, including the transmission of colour signals, and to study recent advances in television technology.
- To gain knowledge of modern consumer electronic devices such as mobile phones, home appliances, and computers, focusing on their applications and technological advancements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Microphones: Introduction, Requirements, Quality of Microphones, Classification, Moving Coil Microphone, Ribbon Microphone, Condenser (or Capacitor) Microphone, Crystal Microphone, Carbon Microphone, Electret Microphone.

Loudspeakers: Introduction, Features of Loudspeaker, Moving Coil (Cone Type) Loudspeaker, Electrodynamic Loudspeaker, Horn Loudspeaker, Loudspeaker for High Fidelity Systems.

(Text : 5.1 to 5.10 and 6.1 to 6.6)

Module-2

Audio Compact Disc Systems: Introduction, Comparison of CD and Tape, Optical Recording, Details of a Compact Disc, Details of Recording Process, Details of playback Process, Geometry of Audio Disc, Encoding Process and Error Correction, D/A Convertor, Handling of Compact Disc.

(Text : 10.1 to 10.10)

Module-3

Colour Television: Introduction, Light Energy, Primary Colours, Tristimulus Values, Trichromatic Coefficients, Colour Triangle, Mixing of Colours, Grassman's Law, Colour Specifications, Bandwidth for Colour Signal Transmission. Chromaticity Diagram, Spectral and Non-Spectral Colours, Colour Circle, Visibility Curve, Digital Television (DTV) and High Definition Television (HDTV), Recent Advances in TV technology, LCD TV, LED TV, Plasma TV

(Text : 14.1 to 14.9, 14.13 to 14.16 and 14.26 to 14.27)

Module-4

	Cable Television: Introduction, Video Monitor, Closed Circuit Television (CCTV), Cable Television, Cable TV Using Internet. **Miscellaneous Devices:** Digital Watch, Calculator, An Electronic Guessing Game, Cordless Telephone. (Text : 15.1 to 15.5 and 17.1 to 17.4)
	Module-5
	Mobile Telephone, Cellular Telephone, UPS, Inverter, Decorative Lighting, Remote Control for TV and VCR, Facsimile (FAX), Pager, Microwave Oven, LCD Timer with Alarm, Electronic Ignition System for Automobiles, Washing Machine, Organisation of Digital computer, Microprocessor, Note Book, Laptop, Tablet PC, Ultrabook, IPAD, Recent Advances in Consumer Electronics. (Text : 17.6 to 17.7 and 17.13 to 17.27)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the functioning and classification of various types of microphones and loudspeakers
2. Demonstrate knowledge of the optical recording and playback processes in audio compact disc systems
3. Analyse the principles of colour television and modern display technologies
4. Evaluate the working of cable television systems and miscellaneous consumer devices
5. Explore advancements in consumer electronics, such as mobile phones, computing devices, and home appliances

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. B.R. Gupta, V. Singhal "Consumer Electronics", S.K. Kataria & Sons, 6th edition, 2013, ISBN 978-93-5014-407-7.
2. R.P.Bali, Consumer Electronics, Pearson Education (2008)

Web links and Video Lectures (e-Resources):

- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview
- Microelectronics: Devices to Circuits: https://onlinecourses.nptel.ac.in/noc24_ee139/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Trouble shoot the common consumer electronics products like T.V., Washing machine , microwave oven , FAX, Copier machine.
- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Make visit to service centres of gadgets covered in curriculum and if possible work there for some days on voluntarily basis during holidays.
- Search internet websites for DYS (Do Your Self) repair of electronic gadgets and try your hands to repair some gadgets based on that.

Electronic Communication Systems		Semester	6
Course Code	BEC654C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Describe essential elements of an electronic communication system.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Define the sampling theorem and methods to generate pulse modulations.
- Learn the various methods of digital modulation techniques and compare the different schemes.
- Introduce the basic concepts of information theory and coding.
- Understand the basic concepts of wireless and cellular communications.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)

Module-2

Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6)

Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)

Module-3

Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)

Module-4

Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5)

Information Theory, Source and Channel Coding: Information, Entropy and its properties, Shannon,- Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]

Module-5

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the scheme and concepts of radiation and propagation of communication signals through air.
2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.
3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.
4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.
5. Compare the different wireless communication systems and describe the structure of cellular communication.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1.
2. 2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Reference Books

1. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1
3. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81- 265-4231-4

Web links and Video Lectures (e-Resources):
1. Communication Engineering **https://nptel.ac.in/courses/117102059**
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning 1. Assignments and test – Knowledge level, Understand Level and Apply level 2. Experiential Learning by using free and open source software's SCILAB or OCTAVE or Python

VISVESVARAYATECHNOLOGICALUNIVERSITY,BELAGAVI
B.E:Electronics & Communication Engineering NEP, OutcomeBasedEducation (OBE)and ChoiceBased CreditSystem(CBCS)
(Effectivefromthe academicyear 2022–23)

VISemester

BasicVLSIDesign			
CourseCode	**21EC654D**	CIEMarks	50
TeachingHours/Week(L:T:P:S)	3:0:0:1	SEEMarks	50
TotalHoursofPedagogy	40	TotalMarks	100
Credits	3	ExamHours	3

Courseobjectives:

- ImpartknowledgeofMOStransistortheoryandCMOStechnologies
- Impartknowledgeonarchitecturalchoicesandperformance trade-offsinvolvedindesigningandrealizingthecircuitsin CMOStechnology
- Cultivatetheconceptsofsubsystemdesignprocesses
- DemonstratetheconceptsofCMOStesting

Teaching-LearningProcess(GeneralInstructions)

Thesamplestrategies,whichtheteachercanusetoacceleratetheattainmentofthevariouscourseoutcomesare listedin thefollowing:

1. Lecturemethod(L)doesnotmeanonlythetraditionallecturemethod,butadifferenttypeofteachin gmethodmaybeadopted todevelop theoutcomes.
2. ShowVideo/animationfilmstoexplainthefunctioningofvarioustechniques.
3. Encouragecollaborative(Group)Learningintheclass
4. AskatleastthreeHOTS(Higher-orderThinking)questionsintheclass,whichpromotescriticalthinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinkingskillssuchastheabilitytoevaluate,generalize,andanalyzeinformationratherthansimplyreca llit.
6. Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeupwiththeirow ncreative ways to solvethem.
7. Discusshoweveryconceptcanbeappliedtotherealworld-andwhenthat'spossible,ithelpsimprovethe students'understanding.
8. IncorporateprogrammingexamplesgivenunderActivitybasedlearning.

Module-1

Introduction:ABrief History,MOS Transistors, MOSTransistor Theory,IdealI-V Characteristics,Non-idealI-VEffects,DCTransferCharacteristics (1.1,1.3,2.1,2.2, 2.4,2.5ofTEXT2).
Fabrication:nMOSFabrication,CMOSFabrication[P-wellprocess,N-wellprocess,Twintubprocess],BiCMOSTechnology (1.7,1.8,1.10of TEXT1).

Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2

Module-2

MOSandBiCMOSCircuitDesignProcesses:MOSLayers,StickDiagrams,DesignRulesandLayout.
BasicCircuitConcepts: SheetResistance,AreaCapacitancesofLayers,StandardUnitofCapacitance, SomeAreaCapacitanceCalculations,DelayUnit,InverterDelays,DrivingLargeCapacitiveLoads(3.1to3.3,4.1,4.3to4.8ofTEXT1).

Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Module-3	
ScalingofMOSCircuits:ScalingModels&ScalingFactorsforDeviceParameters **Subsystem Design Processes**: Some General considerations, An illustration of Design Processes,**Illustration of the Design Processes**: Regularity, Design of an ALU Subsystem, The Manchester Carry-chainandAdderEnhancementTechniques (5.1,5.2, 7.1,7.2,8.2,8.3, 8.4.1,8.4.2 ofTEXT1).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-4	
SubsystemDesign:Some ArchitecturalIssues,SwitchLogic,Gate(restoring)Logic,ParityGenerators,Multiplexers, The ProgrammableLogicArray(PLA) (6.1to6.3,6.4.1,6.4.3,6.4.6 ofTEXT1). **FPGABasedSystems**:Introduction,Basicconcepts,DigitaldesignandFPGAs,FPGAbasedSystemdesign,FPGA architecture, Physical designfor FPGAs(1.1to1.4,3.2,4.8ofTEXT3).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-5	
Memory,RegistersandAspectsofsystemTiming:SystemTimingConsiderations,SomecommonlyusedStorage/Memoryelements(9.1,9.2ofTEXT1). **Testing and Verification**: Introduction, Logic Verification, Logic Verification Principles,ManufacturingTestPrinciples,Designfortestability (12.1,12.1.1, 12.3, 12.5,12.6ofTEXT2).	
Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Courseoutcome(CourseSkillSet)

Attheendofthecoursethestudentwillbeableto:

1. DemonstrateunderstandingofMOStransistortheory,CMOSfabricationflowandtechnologyscaling.
2. Drawthebasicgatesusingthestickandlayoutdiagramswiththeknowledgeofphysicaldesignaspects.
3. InterpretMemoryelementsalongwithtimingconsiderations
4. DemonstrateknowledgeofFPGAbasedsystemdesign
5. InterprettestingandtestabilityissuesinVLSIDesign
6. AnalyzeCMOSsubsystemsandarchitecturalissueswiththedesignconstraints.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A studentshall be deemed to have satisfied the academic requirements and earned the credits allotted to eachsubject/ course if the student secures not less than 35% (18 Marks out of50) in the semester-endexamination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (ContinuousInternalEvaluation)andSEE(Semester End Examination)taken together.

ContinuousInternalEvaluation:

ThreeUnitTestseachof **20Marks(duration01hour**)

1. Firsttestattheendof5thweekofthesemester
2. Secondtestattheendofthe10thweekofthesemester
3. Third test at the end of the 15thweek of the

semesterTwo assignmentseachof**10 Marks**

4. Firstassignmentattheendof4thweek ofthesemester
5. Secondassignmentat theendof9thweekofthesemester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20Marks** (**duration01 hours**)

6. Attheendofthe13th weekofthesemester

Thesumofthreetests,twoassignments,andquiz/seminar/groupdiscussionwillbeoutof100marksandwillbe **scaled downto50marks**

(tohavelessstressedCIE,theportionofthesyllabusshouldnotbecommon/repeatedforanyofthemethodsofth eCIE.Eachmethod ofCIEshouldhaveadifferentsyllabusportionof thecourse).

CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutco me defined for thecourse.

SemesterEndExamination:

TheorySEEwillbeconductedbyUniversityasperthescheduledtimetable,withcommonquestionpapersforthes ubject(**duration 03 hours)**

1. Thequestionpaperwillhavetenquestions.Eachquestionissetfor20marks.
2. Therewillbe2questionsfromeachmodule.Eachofthetwoquestionsunderamodule(withamaximum of3sub-questions),**shouldhaveamixoftopics**underthat module.

The students have to answer 5 full questions, selecting one full question from each module.Marks scoredoutof100shallbe reducedproportionallyto50marks

SuggestedLearningResources:

TextBooks:

1. "BasicVLSIDesign"- DouglasAPucknell&KamranEshraghian,PHI,3rd Edition.
2. "CMOSVLSIDesign-ACircuitsandSystemsPerspective",NeilHEWeste,DavidHarris,AyanBanerjee,3rd Edition,PearsonEducation.
3. "FPGABasedSystemDesign",WayneWolf,PearsonEducation,2004,TechnologyandEngineering.

WeblinksandVideoLectures(e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

Wherevernecessary**Cadence/Synopsis/MentaGraphicstools**mustbeused.

1.WriteVerilogCodeforthefollowingcircuitsandtheirTestBenchforverification,observethewaveform and synthesize the code with technological library with given Constraints*. Do the initialtimingverification withgatelevel simulation.

i. Aninverter
ii. ABuffer
iii. TransmissionGate
iv. Basic/universalgates
v. Flipflop -RS,D, JK,MS, T
vi. Serial&Paralleladder
vii. 4-bitcounter[SynchronousandAsynchronouscounter]

2.Designanop-ampwithgivenspecification*usinggivendifferentialamplifierCommonsourceandCommonDrainamplifieri nlibrary**and completingthedesignflowmentionedbelow:

a. Drawtheschematicandverifythefollowing
   i) DCAnalysis
   ii) ACAnalysis
   iii) TransientAnalysis
b. DrawtheLayout andverifytheDRC,ERC
c. CheckforLVS
d. ExtractRCandbackannotatethesameandverifythe Design.

03.10.2022

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics and Communication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022-2023)

V Semester

NOTE: This Laboratory can be conducted using Industry standard EDA tool like Cadence , Synopsis or any equilent VLSI tool.

VLSI Design and Testing LAB			
Course Code	**BECL606**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

Sl.No.	Experiments
1	Design a 4-Bit Adder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALUBehavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path

	• Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
6	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
7	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increasethe drive strength to 2X and 4X and tabulate the results.

8	Construct the schematic of the Boolean Expression $Y = AB+CD+E$ using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Tabulate the results.
9	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
10	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments (For CIE)

11	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path

12	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record theobservations.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL.
2. Understand the synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
4. Design and simulate basic CMOS circuits like inverter, NOR gate and any Boolean expression .
5. Perform RTL_GDSII flow and understand the stages in ASIC design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shallbe deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubricsfor the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of thepractical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbe evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} weekof the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

03.10.2022

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.
The duration of SEE is 03 hours.
Rubrics suggested in Annexure-II of Regulation book

03.10.2022

FPGA Based System design Lab Using Verilog		Semester	VI
Course Code	**BEC657A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course objectives:

This laboratory course enables students to

- Understand FPGA Design flow for VLSI Chip Design
- Understand the concept of Design and implementation of Advanced Digital System Design
- Learning the Implementation of advanced digital circuits on FPGA boards

	Verilog Program can be compile using any compiler, Verifying the functionality using suitable simulator. Down load the programs on FPGA boards and Verify the Functionality
1	Write a Verilog description for the following combinational logic, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modelling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2	Write a Verilog description for the following Sequential Circuits,Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3	Write a Verilog description for the following Sequential Circuits, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. Ring counter
4	Write a Verilog description for the following Digital Circuits, Verify the functionality usingVerilog test bench and perform the synthesis by downloading the design on to FPGA device. a.4-Bit Ripple Carry Adder b. 4-Bit Linear Feedback shift register
5	Write a Verilog description for the following Digital Circuits, Verify the functionality using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-bitArray Multiplication b. 4-bit Booth Multiplication

6	Write a Verilog description to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality using output device.
7	Interface a Stepper motor to FPGA andWrite a Verilog description to controlStepper motor rotation.
8	Interface a DAC to FPGA and Write a Verilog descriptionto generate Squre wave of frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an output device.
9	Write a Verilog descriptionto convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.

Course outcomes:

- Familiarize with the EDA tool to write HDL programs to understand simulation and synthesis of digital design.
- Design, Simulation and Synthesis of Combinational circuits using EDA tool
- Design, Simulation and Synthesis of Sequential Circuits using EDA tool
- Interfacing DAC to FPGA device to generate different waveforms using Verilog HDL.
- Interfacing Stepper motor to FPGA device to count the number of rotations of a stepper motor.

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Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1) SamirPalnitkar, "Verilog HDL : A guide to digital design and synthesis", Pearson Education, II Edition.

2) Donald E Thomas, Philip R Moorby, "The Verilog hardware description Language", Springer Science Business Media , LLC, 5th Edition

3) Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI),II Edition

4) Padmanabhan, Tripura Sunadri, "Design through Verilog HDL", Wiley, 2016.

5) Verilog HDL user manual

System Modelling using Simulink		Semester	5
Course Code	**BEC657B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination type (SEE)	**Practical**		

Course objectives:

- Understand the basics of MATLAB Simulink used for engineering applications
- Simulation of the trigonometric functions and display of signals.
- Implementations of analog and digital systems using Simulink.
- Implement digital logic circuits using Simulink and display the output.
- Simulation of the analog and digital communication systems using Simulink.

Sl.NO	Experiments
1	a) Generate the following signals using Simulink and display these signals on a single scope with separate inputs. i) sinusoidal signal, ii)square signal, iii) sawtooth signal, and iv) random signal b) Perform the following operations using simulink and display the output. i) y(t) = sin2t, ii) y(t) = $\frac{d(sin2t)}{dt}$, iii)y(t) = $\int sin2t$
2	Solve the second order differential equations shown below using Simulink and display the output. i) $\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + 5y = 1$ ii) $\frac{d^2y}{dt^2} + 3\frac{dy}{dt} + 4y = 5\cos 2t$
3	Design and realize the second order low pass and high pass RC filters using Simulink.
4	Design a BCD adder and use Simulink to simulate and verify its operation.
5	Design and Simulate the following using Simulink and verify its operation. a) 3–bit Up / Down Counter, b) 4–bit Ring Counter
6	Design and simulate the 4x1 Multiplexer and 1x4 Demultiplexer using Simulink
7	Find the step response of the following system functions given below, using Simulink. i) Continuous transfer function H(s) = $\frac{5(s+2)}{s(2s^2+4s+3)}$ ii) Discrete transfer function H(z) = $\frac{z^2-1.2z+1}{z^3-1.3z^2+z-0.2}$
8	Realize the FIR filter given by the impulse response h(n) = {0.08, 0.21,0.54, 0.86, 1, 0.86, 0.54, 0.21 0.08) using Simulink. Obtain the frequency response characteristics.

9	Simulate the Amplitude Modulation and Demodulation using Simulink. Display the output signal and its spectrum.
10	Simulate the modulation & demodulation of a random binary data stream using QPSK using Simulink. Display the output signal and its spectrum.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Create Simulink models to perform analog and digital computations.
- Implement the Combinational Digital circuits and Sequential Digital Circuit models using Simulink.
- Implement analog and digital systems using the transfer functions in s-domain and z-domain respectively.
- Demonstration of analog and digital communication modulation and demodulation using Simulink.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Steven T. Karris, "Introduction to Simulink® with Engineering Applications", Orchard Publications, 2011, ISBN : 978-1934404218
2. Devendra K. Chaturvedi, "Modeling and Simulation of Systems Using MATLAB and Simulink", CRC Press Taylor & Francis Group, 2010, ISBN 9780815351382

IoT (Internet of Things) Lab		Semester	6
Course Code	BEC657C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects.

Sl.No.	Experiments
1(i)	To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds.
1(ii)	To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2 (i)	To interface the DHT11 sensor with Arduino /Raspberry Pi and write a program to print temperature and humidity readings.
2(ii)	To interface OLED with Arduino /Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4(i)	Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.
4(ii)	Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to _thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from _thingspeak _cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.
12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the Internet of Things and its hardware and software components.
- Interface I/O devices, sensors & communication modules.
- Remotely monitor data and control devices.

- Develop real-life IoT-based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands-on Approach", University Press
- Dr. SRN Reddy, Rachit Thukral, and Manasi Mishra, "Introduction to Internet of Things: A Practical Approach", ETI Labs
- Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
- Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
- Adrian McEwen, "Designing the Internet of Things", Wiley
- Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

Python Programming for Machine Learning Applications		Semester	**6**
Course Code	BEC657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge Machine Learning Algorithms
- To develop skills required to build real-life ML Algorithm projects.

Sl.No.	Experiments
1	Solve the Tic-Tac-Toe problem using the Depth First Search technique.
2	Show that the 8-puzzle states are divided into two disjoint sets, such that any state is reachable from any other state in the same set, while no state is reachable from any state in the other set.
3	To represent and evaluate different scenarios using predicate logic and knowledge rules.
4	To apply the Find-S and Candidate Elimination algorithms to a concept learning task and compare their inductive biases and outputs.
5	To construct a decision tree using the ID3 algorithm on a simple classification dataset
6	To assess how the ID3 algorithm performs on datasets with varying characteristics and complexity, examining overfitting, underfitting, and decision tree depth.
7	To examine different types of machine learning approaches (Supervised, Unsupervised, Semi-supervised, and Reinforcement Learning) by setting up a basic classification problem and exploring how each type applies differently
8	To understand how Find-S and Candidate Elimination algorithms search through the hypothesis space in concept learning tasks, and to observe the role of inductive bias in shaping the learned concept.
9	To go through all stages of a real-life machine learning project, from data collection to model fine-tuning, using a regression dataset like the "California Housing Prices."
10	To perform binary and multiclass classification on the MNIST dataset, analyze performance metrics, and perform error analysis.
11	**Demo experiments**
12	Demo experiments

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Apply machine learning algorithms to real life problems.
- Able to make use of different machine learning approaches.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,

Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015

2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.

3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013

4. AurelienGeron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.

Microwave Engineering and Antenna Theory		Semester	7
Course Code	**BEC701**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

This course will enable students to:

1. Describe the microwave properties and its transmission media.
2. Describe the microwave devices for several applications.
3. Understand the basic concepts of antenna theory.
4. Identify antenna types for specific applications.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
3. Adopt Problem Based Learning (PBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
5. Using videos for demonstration of the fundamental principles to students for better understanding of concepts.
6. Demonstration of microwave devices and Antennas in the lab environment where students can study them in real time.

MODULE-1

Microwave Sources: Introduction, Gunn Diode (Text 2: 7.1,7.1.1,7.1.2)

Microwave transmission lines: Microwave frequencies, Microwave devices, Microwave systems. Transmission line equations and solutions, Reflection Coefficient and Transmission Coefficient. Standing wave and standing wave ratio. Smith chart, Single stub matching.

Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 (except double stub matching)

Teaching-Learning Process	Chalk and Talk would be helpful for the quantitative analysis. Videos of the Basic principles of the devices would help students to grasp better. **RBT Level**: L1, L2, L3

MODULE-2

Microwave Network Theory: Introduction, S matrix representation of multi-port networks (Text 1: 6.1, 6.3, 6.3.1, 6.3.2)

Microwave passive devices: Coaxial connectors and Adapters, Attenuators, Phase shifters, waveguide Tees, Magic Tee, Circulator, Isolator. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16, 6.4.17 A, B)

Teaching-Learning	Chalk and Talk, PowerPoint Presentation
MODULE-3	
Strip Lines: Introduction, Microstrip lines, Parallel Strip lines (Text 2: 11.1,11.2) **Antenna Basics**: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam efficiency, Directivity and Gain, Antenna Aperture Effective height, Bandwidth, Radio communication Link, Antenna Field Zones (Text 3: 2.1-2.7, 2.9-2.11, 2.13).	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3
MODULE-4	
Point sources and arrays: Introduction, Point Sources, Power patterns, Power theorem, Radiation Intensity, Arrays of 2 isotropic point sources, Pattern multiplication, Linear arrays of n Isotropic sources of equal amplitude and Spacing. (Text 3: 5.1-5.6, 5.9, 5.13) **Electric Dipole**: Introduction, Short Electric dipole, Fields of a short dipole. Radiation resistance of a short dipole. Thin linear antenna (field analysis). (Text 3: 6.1-6.5)	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3
MODULE-5	
Loop and Horn antenna: Introduction: Small loop, Comparison of far fields of small loop and short dipole. Radiation resistance of small loop, Horn Antennas, Rectangular antennas. (Text 3: 7.1,7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20) **Antenna Types**: Yagi Uda array, Parabolic Reflector, Microstrip Antennas, Features of Microstrip Antennas, (Text 3: 8.8, 9.5, 14.1,14.2)	
Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. RBT Level: L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.
2	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench setup
3	To measure unknown impedance using Smith chart through test bench setup.
4	Study of characteristics of E plane Tee / H plane Tee.
5	Study of characteristics of Magic Tee.
6	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
7	Coupling and Isolation characteristics of microstrip directional coupler.
8	Determination of power division of microstrip power divider.
9	To plot a 2D and 3D radiation pattern of dipole Antenna (Use any simulation software)
10	Obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to transmission lines.
3. Identify microwave devices for several applications.
4. Analyze various antenna parameters and their significance in building the RF system.
5. Identify various antenna configurations for suitable applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Text Books:

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2ndEdition, 2010.
2. Microwave Devices and Circuits – Samuel Y Liao, Pearson Education.
3. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013.

Reference Books:

1. Microwave Engineering -David M Pozar, John Wiley India Pvt Ltd., Pvt Ltd., 3rd edition, 2008.
2. Microwave Engineering-Sushrut Das, Oxford Higher Education, 2nd Edn, 2015.
3. Antennas and Wave Propagation- Harish and Sachidananda, Oxford University Press, 2007.

Web links and Video Lectures (e-Resources):

1. https://www.tutorialspoint.com/antenna_theory/antenna_theory_horn.html
2. http://www.antenna-theory.com/antennas/smallLoop.php

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve practical skills

COMPUTER NETWORKS & PROTOCOLS
B.E., VII Semester, Electronics & Communication Engineering [As per Choice Based Credit System (CBCS) Scheme]

Course Code	BEC702	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

*Understand the layering architecture of OSI reference model and TCP/IP protocolsuite.

*Understand the protocols associated with each layer.
*Learn the different networking architectures and their representations.
* Learn the various routing techniques and the transport layer services.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.. Network Models: TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP(1.1,1.2, 1.3.1to 1.3.4,2.2, 2.3 ,9.1, 9.2.1, 9.2.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Data Link Control (DLC) services: Framing, Flow and Error Control. Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Connecting Devices: Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches, Advantages. Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control. (11.1,12.1,13.1, 13.2.1 to 13.2.5,15.1,17.1,17.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. IPv6 addressing and Protocol. Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. (18.1(excluding 18.1.3), 18.2, 18.4,19.1,20.1, 20.2,22.1 and 22.2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol, Piggybacking Transport-Layer Protocols in the Internet: User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Error control, TCP congestion control. (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4, 23.2.5,24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.6, 24.3.8, 24.3.9)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client Server Protocols: Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. Quality of Service (25.1, 26.1.2, 26.2, 26.3, 26.6, 30.1, 30.2.)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following :

Sl.No	Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet or any other equivalent tool
1	Implement a point to point network with four nodes and duplex links between them.Analyze the network performance by setting the queue size and varying the bandwidth.
2	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3.Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine thenumber of packets sent by TCP/UDP.
3	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes andobtain congestion window for different sources/ destinations.
5	Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6	Implementation of Link state routing algorithm
Implement the following using programming languages C/C++ etc,.	
7	Write a program for a HLDC frame to perform the following. i) Bit stuffing ii) Character stuffing.
8	Write a program for distance vector algorithm to find suitable path for transmission
9	Implement Dijkstra‘s algorithm to compute the shortest routing path.
10	For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify theprogram for the cases : i)with out error ii)with error
11	Implementation of Stop and Wait Protocol and Sliding Window Protocol
12	Write a program for congestion control using leaky bucket algorithm.

Course Outcomes

At the end of the course the student will be able to:

1. Understand the concepts of networking thoroughly.
2. Identify the protocols and services of different layers.
3. Distinguish the basic network configurations and standards associated with each network.
4. Discuss and analyze the various applications that can be implemented on networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Book:

Data Communications and Networking, Forouzan, 5th Edition, McGraw Hill, 2016 ISBN: 1-25-906475-3

Reference Books:

1.A.S Tanenbaum - Computer Networks, 4th Edition, PHI, 2003
2.Computer Networks, James J Kurose, Keith W Ross, Pearson Education,2013, ISBN: 0-273-76896-4
3.Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

Wireless Communication Systems		Semester	5
Course Code	BEC703	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Understand the concepts of signal propagation over wireless channels
- Understand the multiple access techniques used in cellular communications standards.
- Understand the system architecture and layers of LTE based on the use of OFDMA and SC-FDMA principles.
- Understand the design and coding of MIMO wireless systems .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Principles of Wireless Communications: The Wireless Communication Environment, Modelling of wireless systems, System model for narrowband Signals, Rayleigh fading Wireless Channel.

The Wireless Channel: Basics of Wireless Channel Modelling, Average Delay Spread in Outdoor Cellular Channels, Coherence bandwidth, Relation between ISI and Coherence Bandwidth, Doppler fading, Doppler Impact on a wireless Channel, Coherence Time.

[**Text1:** 3.1 to 3.4, 4.1 to 4.7]

Module-2

Code Division for Multiple Access (CDMA): Basic CDMA Mechanism, Fundamentals of CDMA codes, Spreading Codes based on PN sequences, Correlation Properties of Random CDMA Spreading Sequences, Advantages of CDMA.

Orthogonal Frequency Division Multiplexing (OFDM): Introduction, Motivation and Multicarrier basics, OFDM basics, OFDM Example, MIMO OFDM, OFDM Peak to Average Power ratio, SC-FDMA.

[**Text1:** 5.1 to 5.5, 5.7, 7.1, 7.2, 7.3, 7.5, 7.7, 7.8]

Module-3

Evolution of Cellular Technologies: First Generation Cellular Systems, 2G Digital cellular systems – GSM and its Evolution, 3G Broadband Wireless Systems, Key Enabling Technologies and features of LTE, LTE Network Architecture.

Frequency Domain Multiple Accesses: Multiple Access for OFDM Systems, Orthogonal Frequency Division Multiple Access, Single Carrier Frequency Division Multiple Access.

[Text2: 1.2.1, 1.2.1.1, 1.2.2, 1.2.2.1, 1.2.3 (Only the mentioned sections and subsections), 1.4, 1.5, 4.1, 4.2, 4.3]

Module-4

Multiple Input Multiple Output Wireless Communications: Introduction to MIMO Communications, MIMO system Model, MIMO Zero Forcing Receiver, MIMO MMSE Receiver, Singular Value decomposition of MIMO Channel, SVD and MIMO capacity, Alamouti and Space-Time Codes, Nonlinear MIMO receiver: V-Blast, MIMO Beamforming.
[Text1:6.1,6.2, 6.3, 6.4, 6.5, 6.6, 6.8, 6.9, 6.10]

Module-5

Overview and Channel Structure of LTE: Radio Interface Architecture, LTE Design principles, Network Architecture, Radio Interface Protocols, Hierarchical Structure of LTE: Logical Channels, transport Channels and Physical Channels, Channel mapping, Downlink OFDMA Radio resources, Physical Resource Blocks for OFDMA, Uplink SC-FDMA Radio resources.
[**Text2:** 6.1 to 6.4]

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the wireless channel models for slow and fast fading environment.
2. Understand the different multiple access technologies used in wireless communications.
3. Understand the system architecture and the functional standard specified in LTE 4G.
4. Describe the of MIMO transmitter and receiver process using coding examples.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. Aditya K Jagannatham, "Principles of Modern Wireless Communication systems, Theory and Practice ", Mc Graw Hill Education (India) Private Limited, 2017, ISBN 978-81- 265-4231-4.
2. Arunabha Ghosh, Jun Zhang, Jeffrey G. Andrews, Rias Muhamed, "Fundamentals of LTE", Pearson India Education Services Private Limited, 2018, ISBN: 978-93-530-6239-2.

Reference Books

1. T L Singal, "Wireless Communications", Mc Graw Hill Education (India) Private Limited, 2016, ISBN:978-0-07-068178-1
2. Theodore Rappaport, Wireless Communications: Principles and Practice, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.

3. Gary Mullet, Introduction to Wireless Telecommunications Systems and Networks, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Web links and Video Lectures (e-Resources):

1. **Advanced 3G and 4G wireless Mobile Communications:**

   https://nptel.ac.in/courses/117104099

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open source software's OCTAVE or Python

Application Specific Integrated Circuit			
Course Code	**BEC714A**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03(Theory)

Course Learning objectives: This course will enable students to:

- Understand the ASIC design methodologies and programmable logic cells to implement a function on IC.
- Analyze the back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Understand performance evaluation parameters in FPGA and ASIC VLSI chip designs.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

Text 1: [1.1,1.2,1.5,2.6,2.7,2.8]

RBT Levels: L2

Module-2

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design.
Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

Text 1: [3.3,3.4,5.1,5.2,5.3,5.4]

RBT Levels: L2, L3

Module-3

Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

Text 1: [9.1,15.2, 15.3, 15.4,15.7]

RBT Levels: L2, L3

Module-4

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

Text 1: [16.1,16.2,16.3]

RBT Levels: L2, L3

Module-5

Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

Text 1: [17.1,17.2,17.3 , 17.4]

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Text Books:

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005

2. Khosrow Golshan Conexant Systems, Inc. 2007 Springer Science Business Media " Physical Design Essentials " An ASIC Design Implementation Perspective

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective" , Addison Wesley/ Pearson education 3rdedition, 2011
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
3. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

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Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**
- **Real world Problem Solving: Applying the ASIC front end and backend concepts.**

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl.No	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort	L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition , routing using algorithms and EDA tools	L3,L4
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L3 ,L4

B. E. Electronics and Communication Engineering
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

Computer and Network Security

Course Code	BEC714B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100

CREDITS – 03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services, Vulnerabilities in the host machines.
- Core Competence: To equip students with a basic foundation on computer as well as network security by delivering the basics of malicious software, intrusion detection, vulnerability Analysis, auditing as well as securities related to network, system, user and programs

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1	RBTL Level
Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. **(Text2: Chapter1)** Security Mechanisms, Services and Attacks, A model for Network security **(Text1: Chapter1: 3, 4, 5, 6)**	L1, L2, L3
MODULE-2	
Malicious Logic: Introduction, Trojan Horses, Computer Viruses, Computer Worms, Other Forms of Malicious Logic, Defenses (Text 3: Chapter 12) **Vulnerability Analysis:** Introduction, Penetration Studies, Vulnerability Classification, Frameworks (Text 3: Chapter 13)	L1, L2, L3
MODULE-3	

Auditing: Definitions, Anatomy of an Auditing System, Designing an Auditing System, A Posterior Design, Auditing Mechanisms, Examples, Audit Browsing (Text 3: Chapter 14) **Intrusion Detection**: Principles, Basic Intrusion Detection, Models, Architecture, Organization of Intrusion Detection Systems, Intrusion Response (Text 3: Chapter 15)	L1, L2, L3
MODULE-4	
Network Security: Introduction, Policy Development, Network Organization, Availability and Network Flooding, Anticipating Attacks (Text 3: Chapter 16) **System Security:** Introduction, Policy, Networks, Users, Authentication, Processes, Files, Retrospective (Text 3: Chapter 17)	L1, L2, L3
MODULE-5	
User Security: Policy, Access, Files and Devices, Processes, Electronic Communications (Text 3: Chapter 18) **Program Security:** Introduction, Requirements and Policy, Design, Refinement and Implementations (Text 3: Chapter 19: Section 1, 2, 3, 4)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the various types of attacks on computer and network security from malicious logic and intruders.
- Explain how to analyze the various vulnerabilities in the system which can compromise the security.
- Explain how auditing is essential to detect intrusion or suspicious activities in the system.
- Explain the process involved to provide security with respect to network, system, user and program.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.
3. Matt Bishop, Sathyanarayana S Venkatramanayya, "Introduction to Computer Security", Pearson Education, 2006, ISBN 81-7758-425-1

Reference Books

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

Automotive Electronics		Semester	7
Course Code	**BEC714C**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features
- Design and implement the electronics that attribute the reliability, safety, and smartness to automobile, providing add – on comforts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain the functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' analytical skills and develops design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to devise creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive systems, The Engine- Engine Block, Cylinder Head, four stroke Cycle, Engine Control, Ignition System- Spark plug, High voltage circuit and distribution, spark pulse generation, ignition timing, diesel engine, Drive Train – Transmission, drive shaft, differential, suspension, brakes, steering system, starter battery-operating principle. **(Text1: Chapter1, Text 2: Pg. 407-410)**

The Basics of Electronic Engine Control - Motivation for Electronic Engine, control – exhaust emissions, fuel economy, concept of an electronic engine, control system, definition of general terms, definition of engine performance terms, engine mapping, effect of air/fuel ration, spark timing and EGR on performance, control strategy, electronic fuel control system, analysis of intake manifold pressure, electronic ignition. **(Text1: Chapter 5)**

Module-2
Automotive Sensors – Automotive control system applications of sensors and Actuators – Variables to be measured, airflow rate sensor, strain gauge MAP sensor, Hall Effect position sensor, Magnetic Reluctance Crankshaft position sensor, Throttle angle sensor, Engine coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2 /EGO) Lambda sensors, piezoelectric Knock sensor **(Text 1: Chapter 6)** **Automotive Engine Control Actuators** – Solenide, Fuel Injector, EGR actuator, Ignition system **(Text 1: Chapter 6)**
Module-3
Digital Engine Control System- Digital Engine control features, Control modes for fuel control (Seven Modes), EGR Control, Electronic Ignition control- closed loop ignition timing, spark advance correction scheme, Integrated engine control system- secondary air management, Evaporative Emissions, Canister Purge, automatic system adjustment, system diagnostics **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data Processing, Programming, Digital modules in the Control Unit, Control Unit Software **(Text 2: Pg. 196-207)**

Module-4
Automotive Networking – Bus Stem- classification, Applications in the Vehicle, Coupling of networks, Examples of Networked Vehicles **(Text 2: Pg. 85-91),** **Buses** – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces **(Text 2: Pg. 92-151)** **Vehicle Motion Control –** Typical Cruise control system, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Cruse Control Configuration, Cruise Control Electronics (Digital Only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**
Module-5
Automotive Diagnostics – Timing Light, Engine Analyzer, On-Board diagnostics, Off-Board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag Systems **(Text1: Chapter10)** **Future Automotive Electronic Systems –** Alternative Fuel Engines, Electric and Hybrid Vehicles, Fuel Cell Power Cars, Collision Avoidance Radar Warning Systems, Low tire pressure warning systems, Head Up Display, Speech Synthesis, Navigation- Navigation Sensors – Radio Navigation, Signpost Navigation, Dead reckoning navigation, Voice Recognition Cell phone Dialing, Advanced Cruise Control, Stability Augmentation, Automatic Driving Control **(Text 1: Chapter 11)**
Course Outcome (Course Skill Set) At the end of the course, students will be able to: • Describe the basics of Automobile dynamics and design electronics. • Acquire an overview of automotive components, subsystems and basics of Electronic Engine Control in today's automotive industry. • Use available automotive sensors and actuators while interfacing with microcontrollers/microprocessors during automotive system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. **William B Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.**
2. **Robert Bosch GmbH (Ed.), "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", 5th edition, John Wiley & Sons Inc., 2007.**

Web links and Video Lectures (e-Resources):
Related NPTEL Courses

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving using group discussion.
- Present animation for Car assembly
- Real world example of Automotive Electronics concepts.

	Radar Communication	Semester	5
Course Code	BEC714D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives: This Course will enable the students to

- Understand the concepts of Radar, types of Radar and Applications.
- Understand the various measurements in Radar and Propagation of waves.
- Understand the various types of Radar and its functions.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to RADAR: Basic Radar, Simple Radar equation, Radar Block diagram, Radar Frequencies, Applications of Radar.

The RADAR Equation: Detection of signals in Noise, Receiver Noise and SNR, Integration of Radar Pulses, Radar Cross section of Targets, Radar Cross section Fluctuations, Transmitter Power, Pulse Repetition Frequency, Antenna parameters, System Losses.

[**Text1:** 1.1 to 1.5, 2.2, 2.3, 2.6 to 2.12]

Module-2

MTI and Pulse Doppler Radar: Introduction to Doppler and MTI Radar, Delay-Line Cancelers, Moving Target Detector, Pulse Doppler radar.

Tracking Radar: Tracking with Radar, Mono-pulse tracking, Conical Scanning and Sequential Lobing, Tracking in Range, Comparison of Trackers.

[**Text1:** 3.1, 3.2, 3.6, 3.9, 4.1, 4.2, 4.3, 4.6, 4.8]

Module-3

Information from Radar Signals: Introduction, Basic Radar Measurements, Accuracy of measurements.

Radar Clutter: Introduction, Surface-Clutter Radar equation, Land clutter sea Clutter.

Propagation of Radar Waves: Introduction, Scattering from Flat Earth, Scattering from the Round Earth's Surface, Atmospheric Refraction.

[Text1: 6.1, 6.2, 6.3, 7.1 to 7.4, 8.1 to 8.4.]

Module-4

Radar Transmitters: Introduction, Linear beam power tubes, solid state RF power sources.
Radar Receiver: Fundamentals, Receiver Noise Figure, Super heterodyne receiver, Duplexer.
[Text1: 10.1, 10.2, 10.3, 11.1 to 11.4]

Module-5

Synthetic Aperture Radar (SAR): Introduction, SAR History, General Description – Resolution, SAR Signal processing, Radar Equation of the SAR system, SAR system Design considerations.
Over-the-Horizon Radar (OTHR): Introduction, Classification, Ionospheric effects, Ray path trajectories, Principles of OTHR systems.
Secondary Surveillance Radar: Introduction, Principles of SSR, Deficiencies in SSR, Solution to deficiencies, Range performance in SSR.
[**Text-2:** 9.1 to 9.6, 14.3 to 14.6, 15.1 to 15.5]

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the principles of Radar.
2. Analyze the tracking in radar and modelling of Radars.
3. Analyze the limitations, interference and propagation of Radar waves.
4. Describe the Radar transmitter and receiver, and modern Radars.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Merrill L. Skolnik, "Introduction to RADAAR Systems", 3rd edition, Mc Graw Hill Education (India) Private Limited, 2016 (Reprint), ISBN 978-0-07-044533-8.
2. Habibur Rahman, "Fundamental Principles of RADAR", CRC Press, 2019, ISBN: 978-1-138-38779-9.

Reference Books

1. Mark A Richards, James A. Scheer, William A. Holm, "Principles of Modern RADAR", Yesdee Publishing Private Ltd, , 2012, ISBN: 978-93-80381-29-9.
2. Bassem R. Mahafza, " Radar Systems Analysis and Design using MATLAB", 4th edition, CRC press, 2022, ISBN 978-0-367-50793-0.
3. J.C. Toomay, Paul J. Hannen; "Principles of Radar", Third Edition, PHI Learning Pvt Ltd., 2011, ISBN : 978-81-203-4155-9.

Web links and Video Lectures (e-Resources):

1. **NPTEL : Radar Principles**

   https://archive.nptel.ac.in/courses/108/105/108105154/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open source software's OCTAVE or Python
2. Experiential Learning / Simulation using MATLAB.

E-Waste Management		Semester	7
Course Code	**BEC 755A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- **Understanding e-waste**: To learn about e-waste, its different types, and how it's generated
- **E-waste rules and directives**: To understand the rules and directives for e-waste in different countries
- **E-waste management**: To learn how to manage e-waste throughout its life cycle
- **Environmental and health impacts**: To understand the environmental and health impacts of e-waste

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Preamble, What is e-waste, E-waste Sources and generation, Growth of Electrical and Electronics Industry in India, Global Context of e-waste Management, Indian Scenario on e-waste Management,

E-WASTE: E-waste Definition, Classification of e-waste, Characterization of e-waste

Text 1: Chapter 1 & 2

Module-2

Regulatory Framework: Global e-waste Regulations, Waste Electronics and Electrical Equipment (WEEE Directive 82), International norms – Basel Convention, Evolution of e-waste regulations in India, E-waste Management Rules 2016 (amendments to 2011 Rules), Regulatory Compliance Mechanisms, E-waste Management Guidelines (Text 1: 3.1 to 3.7)

Module-3

Extended Producer Responsibility (EPR): E-waste – A post Consumer Waste, E-waste value Chain, E-waste Collection Systems, Extended Producer Responsibility (EPR), Collective Responsibility, Producer Responsible Organization (PRO) (Text 2: 4.1 to 4.6)

Module-4

E-Waste Handling: Characterization & Classification, Packaging and Labelling, Transportation, Storage, Safety in Handling – Precautionary Principles: Text 1- Chapter 5

Module-5

Restrictions on Use of Hazardous Substances (ROHS): Hazardous substances in e-waste, Global ROHS compliances (ROHS Directive 84), ROHS compliance requirements in India: Text 1: Chapter 6

E-Waste Recycling: E-waste Recycling Operations, Dismantling & Segregation, Recycling & Recovery, Recycling Technologies – Text 1: Chapter 7 (7.1 to 7.4)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the environmental impacts of e-waste
2. Distinguish the role of various national and internal act and laws applicable for e-waste management and handling
3. Analyse the e-waste handling methods & restrictions
4. Analyze the e-waste recycling techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. Lakshmi Raghupathy, Introduction to E-Waste Management, TERI Press, New Delhi

Reference Books:

1. Johri R., E-waste: implications, regulations, and management in India and current global best practices, TERI Press, New Delhi

Web links and Video Lectures (e-Resources):

- https://news.mit.edu/2013/ewaste-mit

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for the generated e-waste and its management and prepare a report
- Field visit to explore the possibility of various e-waste management techniques

Automotive Engineering		Semester	7
Course Code	**BEC755B**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features
- Design and implement the electronics that attribute the reliability, safety, and smartness to automobile, providing add – on comforts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain the functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' analytical skills and develops design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to devise creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive systems, The Engine- Engine Block, Cylinder Head, four stroke Cycle, Engine Control, Ignition System- Spark plug, High voltage circuit and distribution, spark pulse generation, ignition timing, diesel engine, Drive Train – Transmission, drive shaft, differential, suspension, brakes, steering system, starter battery-operating principle. **(Text1: Chapter1, Text 2: Pg. 407-410)**

The Basics of Electronic Engine Control - Motivation for Electronic Engine, control – exhaust emissions, fuel economy, concept of an electronic engine, control system, definition of general terms, definition of engine performance terms, engine mapping, effect of air/fuel ration, spark timing and EGR on performance, control strategy, electronic fuel control system, analysis of intake manifold pressure, electronic ignition. **(Text1: Chapter 5)**

Module-2
Automotive Sensors – Automotive control system applications of sensors and Actuators – Variables to be measured, airflow rate sensor, strain gauge MAP sensor, Hall Effect position sensor, Magnetic Reluctance Crankshaft position sensor, Throttle angle sensor, Engine coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2 /EGO) Lambda sensors, piezoelectric Knock sensor **(Text 1: Chapter 6)** **Automotive Engine Control Actuators** – Solenide, Fuel Injector, EGR actuator, Ignition system **(Text 1: Chapter 6)**
Module-3
Digital Engine Control System- Digital Engine control features, Control modes for fuel control (Seven Modes), EGR Control, Electronic Ignition control- closed loop ignition timing, spark advance correction scheme, Integrated engine control system- secondary air management, Evaporative Emissions, Canister Purge, automatic system adjustment, system diagnostics **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data Processing, Programming, Digital modules in the Control Unit, Control Unit Software **(Text 2: Pg. 196-207)**

Module-4

Automotive Networking – Bus Stem- classification, Applications in the Vehicle, Coupling of networks, Examples of Networked Vehicles **(Text 2: Pg. 85-91),**
Buses – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces **(Text 2: Pg. 92-151)**

Vehicle Motion Control – Typical Cruise control system, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Cruise Control Configuration, Cruise Control Electronics (Digital Only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**

Module-5

Automotive Diagnostics – Timing Light, Engine Analyzer, On-Board diagnostics, Off-Board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag Systems **(Text1: Chapter10)**

Future Automotive Electronic Systems – Alternative Fuel Engines, Electric and Hybrid Vehicles, Fuel Cell Power Cars, Collision Avoidance Radar Warning Systems, Low tire pressure warning systems, Head Up Display, Speech Synthesis, Navigation- Navigation Sensors – Radio Navigation, Signpost Navigation, Dead reckoning navigation, Voice Recognition Cell phone Dialing, Advanced Cruise Control, Stability Augmentation, Automatic Driving Control **(Text 1: Chapter 11)**

Course Outcome (Course Skill Set)

At the end of the course, students will be able to:

- Describe the basics of Automobile dynamics and design electronics.
- Acquire an overview of automotive components, subsystems and basics of Electronic Engine Control in today's automotive industry.
- Use available automotive sensors and actuators while interfacing with microcontrollers/microprocessors during automotive system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. **William B Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.**
2. **Robert Bosch GmbH (Ed.), "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", 5th edition, John Wiley & Sons Inc., 2007.**

Web links and Video Lectures (e-Resources):
Related NPTEL Courses

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving using group discussion.
- Present animation for Car assembly
- Real world example of Automotive Electronics concepts.

	Embedded Systems Applications		Semester	7
	Course Code	**BTE755C**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- Understand the fundamental concepts, characteristics, and applications of embedded systems across various domains.
- Analyse the hardware components of embedded systems, including microcontrollers, memory, and low-power design techniques.
- Explore the role of sensors, ADCs, and actuators in embedded systems, and their interfacing with digital systems.
- Apply embedded systems design principles in real-world applications such as mobile phones, automotive electronics, RFID, and biomedical systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to embedded systems: Application domain of embedded systems, desirable features and general characteristics of embedded systems, model of an embedded system, microprocessor Vs microcontroller, example of a simple embedded system, figure of merit for an embedded system, classification of MCUs: 4/8/16/32 bits, history of embedded systems, current trends.

(Text: 1.1 to 1.9)

Module-2

Embedded systems-The hardware point of view: Microcontroller unit (MCU), The Processor, The Harvard Architecture, A popular 8-bit MCU: General Purpose I/O (GPIO), Clock; Memory for embedded systems: Semiconductor Memory, Random Access Memory (RAM), Static RAM (SRAM), An SRAM Chip. Low Power Design, Pull up and Pull Down Resistors.

(Text: 2.1 to 2.2.2, 2.3 to 2.3.2.2 and 2.4 to 2.5)

Module-3

Sensors, ADCs and Actuators

Sensors: Temperature Sensor, Light Sensor, Proximity/range Sensor; Analog to digital converters: ADC Interfacing, Control Interface, Data Interface; Actuators: Displays, Light Emitting Diodes (LED), Seven Segment LED; Motors: Stepper Motors, DC Motors.

(Text: 3.1.1 to 3.1.3, 3.2 to 3.2.1.2, 3.3 to 3.3.1.2 and 3.3.2 to 3.3.2.2)

Module-4

	Examples of embedded systems: Mobile phone, Automotive electronics, Radio Frequency Identification (RFID), Wireless Sensor Networks (WISENET), Robotics, Biomedical applications, Brain machine interface. (Text: 4.1 to 4.7)
	Module-5
	Embedded Design-A Systems Perspective: A Typical Example, Product Design, The Design Process, Testing, Bulk Manufacturing. (Text: 18.1 to 18.5)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the fundamental concepts and characteristics of embedded systems, including their classification and modern trends.
2. Analyse the architecture and hardware components of MCUs and their role in embedded systems.
3. Apply knowledge of sensors, ADCs, and actuators for interfacing and control in embedded systems.
4. Evaluate real-world embedded system applications such as mobile phones, automotive electronics, RFID, and robotics.
5. Develop an understanding of the embedded design process, from concept to bulk manufacturing, including testing and product design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Das, LyLa B.. Embedded Systems: An Integrated Approach. India: Pearson Education India, ISBN 9788131787663, 2013.

Web links and Video Lectures (e-Resources):

- Embedded Systems: https://nptel.ac.in/courses/108102045
- Embedded Systems Design: https://onlinecourses.nptel.ac.in/noc20_cs14/preview
- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Students can interface a temperature sensor with an ADC and display the digital output on a seven-segment display, demonstrating sensor integration with actuators.

	Sensors and Actuators	Semester	7
Course Code	**BEC755D**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- To provide the fundamental knowledge about sensors and measurement system.
- To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.
- To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.
- To discuss basics of signal conditioning and signal conditioning equipment.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical Thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Sensors and Transducers: Introduction, Definition of Sensors and Transducers, Classification of Transducers, Advantages and Disadvantages of Electrical Transducers. **(Text 1:16.1 to 16.4)**

Measurement: Introduction to measurement and Instrumentation, Definition, significance of Measurement, Methods of measurement, Modes of measurement, Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, Applications of measurement systems. **(Text 1:3.1 to 3.7)**

Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation. **RBT Level:** L1, L2, L3

Module-2

Static and Dynamic Characteristics of instruments: Introduction, Definition relating to measuring instruments.

Static characteristics - Accuracy, Errors and Correction, Static calibration Range and span. Scale readability Repeatability and Reproducibility, Drift, Accuracy and Precision, Sensitivity, Linearity, Hysteresis, Threshold and Resolution, Dead Zone and Dead Time, Loading Effects and Noise.

Dynamic Characteristics– Dynamic Response, Dynamic characteristics of a measurement system, Dynamic analysis of a measurement system, Zero, First and Second order system.

(Text 1: 3.8, 3.8.1 to 3.8.4.4)

Teaching-Learning Process	Chalk and Talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Measurement of Temperature: Introduction, Temperature measuring instruments, RTD, Thermistors, Thermocouple Thermometers, Radiation Pyrometers, Optical Pyrometers. **(Text 1: 21.2, 21.2.1 to 21.2.7)** **Measurement of Displacement:** Introduction, Principles of Transduction –Variable resistance devices, Variable Inductance Transducer, Induction Potentiometers, Synchros and Resolvers, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer. **(Text 2: 4, 4.1 to 4.3)**	
Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors **RBT Level:** L1, L2, L3
Module-4	
Measurement of Strain: Introduction, Factors affecting strain measurements, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges, Thin film Guages (principle, types & list of characteristics only), Strain gauge Circuits – Wheatstone bride circuit, Applications. **(Text 2: 5, 5.1 to 5.5, 5.8, 5.8.1, 5.10)** **Measurement of Force & Torque:** Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. **Torque measurement:** Absorption type, transmission type, stress type & deflection type. **(Text 2: 10.1,10.2,10.2.1,10.2.2,10.2.3,10.2.6,10.7,10.8,10.9)**	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors **RBT Level:** L1, L2, L3
Module-5	
Signal Condition: Introduction, Functions of Signal Conditioning Equipment, Amplification, Types of Amplifiers, Mechanical Amplifiers Fluid Amplifiers, Optical Amplifiers, Electrical and electronic Amplifiers. **(Text 1: 17.1 to 17.8)** **Data Acquisition Systems and Conversion:** Introduction, Objectives and Configuration of Data Acquisition System, Data Acquisition Systems, Data Conversion. **(Text 1: 18.1 to 18.4)**	
Teaching-Learning Process	Chalk and Talk method, PowerPoint Presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system.
2. Interpret and analyse the static and dynamic characteristics of instruments.
3. Elucidate the working principle and usage of different transducers for temperature, and displacement measurement.
4. Discuss the principle and working of strain, force and torque measurement.
5. Analyze the signal conditioning and signal conditioning equipment.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(To have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Electrical and Electronic Measurements and instrumentation, R.K Rajput, S. Chand, 4th Edition, 2015.
2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2nd Edition (32 Reprint), McGraw Hill Education (India), 2014.

Reference Books :

1. Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17th Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004.
2. A Course in Electronics and Electrical Measurements and Instruments, J.B. Gupta, Katson Books, 13th Edition, 2008.